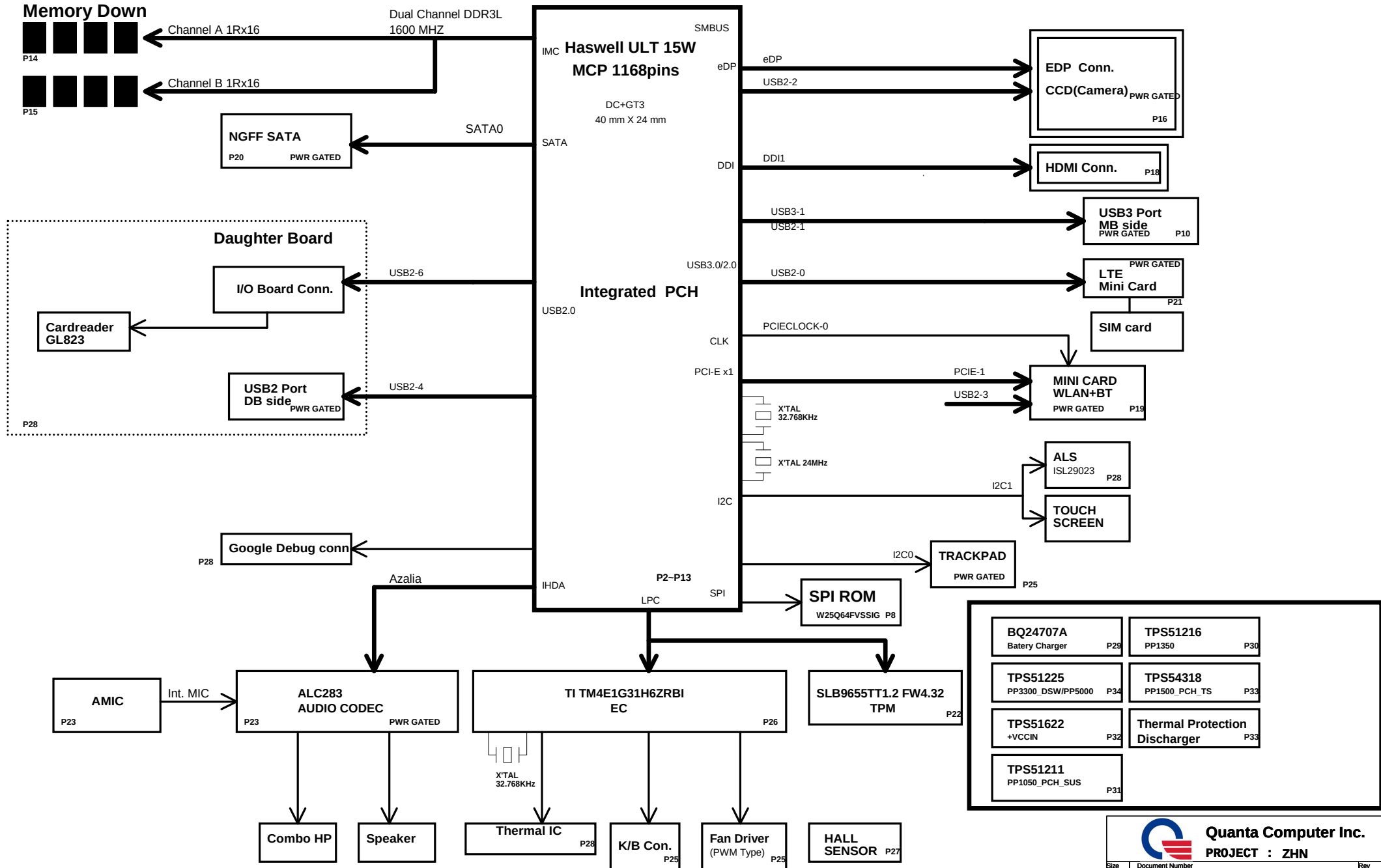


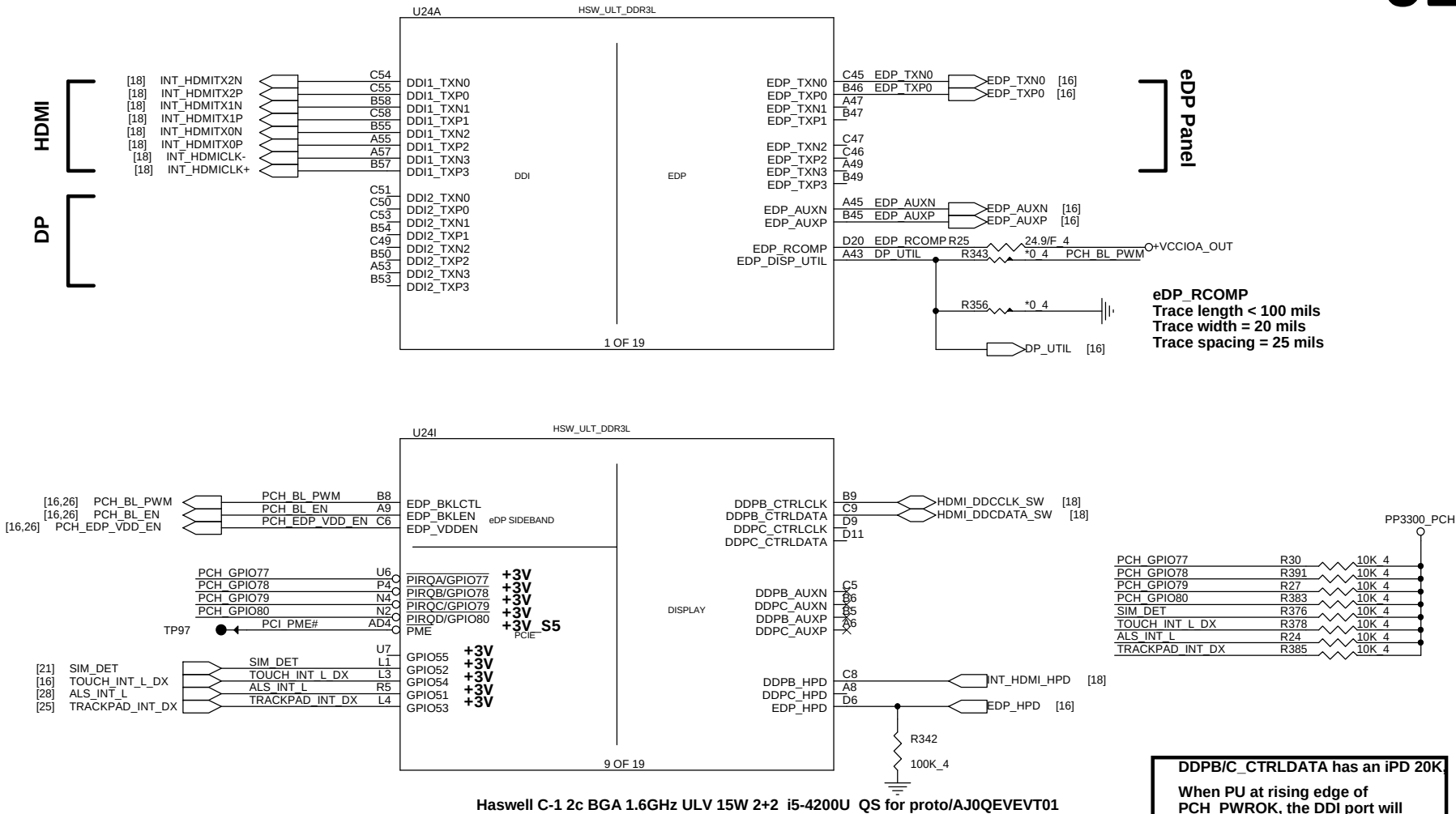
ZHN SHB ULT SYSTEM BLOCK DIAGRAM

01



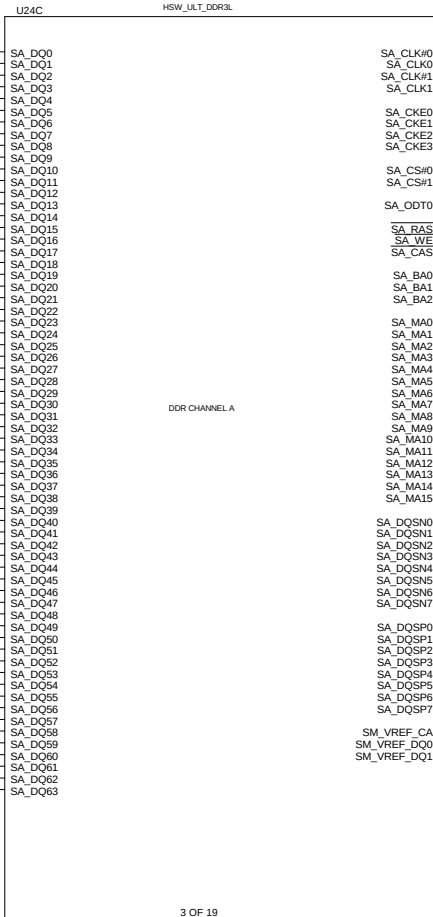
Haswell ULT (DISPLAY, eDP)

02



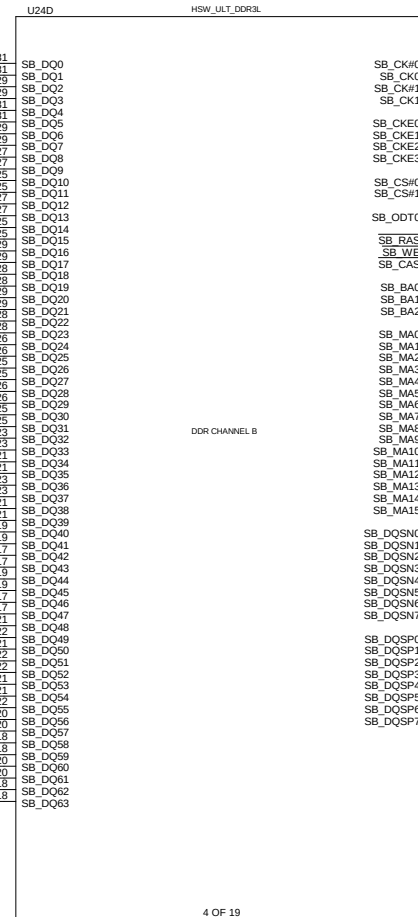
DDPB/C_CTRLDATA has an iPD 20K.
When PU at rising edge of PCH_PWROK, the DDI port will be detected

Haswell ULT (DDR3L)



3 OF 19

Haswell Processor (DDR3L)



4 OF 19

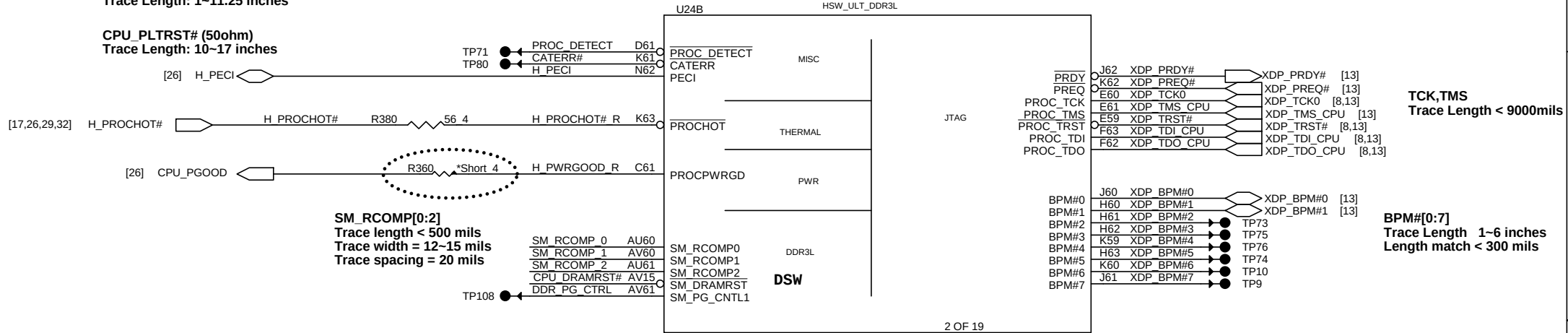
03

Haswell ULT (SIDE BAND)

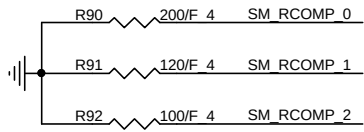
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

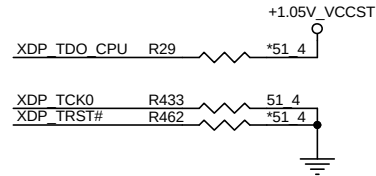
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



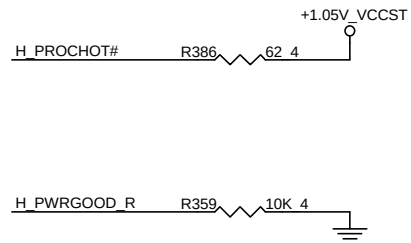
DRAM COMP



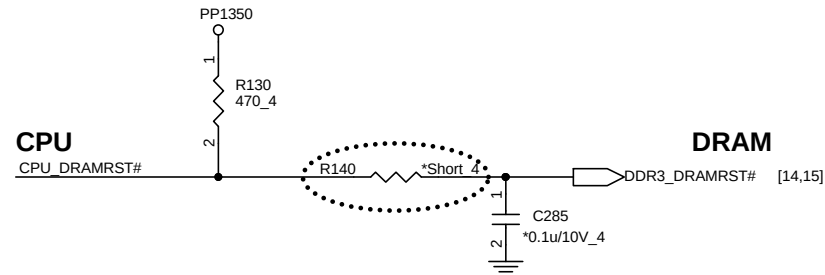
XDP PU/PD



PU/PD of CPU



DRAMRST



05

6/21 Add C384~C388 by Intel DDR.

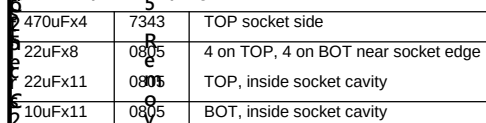


**Place PU resistor
close to CPU**

**Place PU resistor
close to CPU**

H CPU SVIDART# R389 43 4 VR_SVID_ALERT# [32]

H CPU SVIDCLK R388 *Short 4 VR_SVID_CLK [32]

**Quanta Computer Inc.**

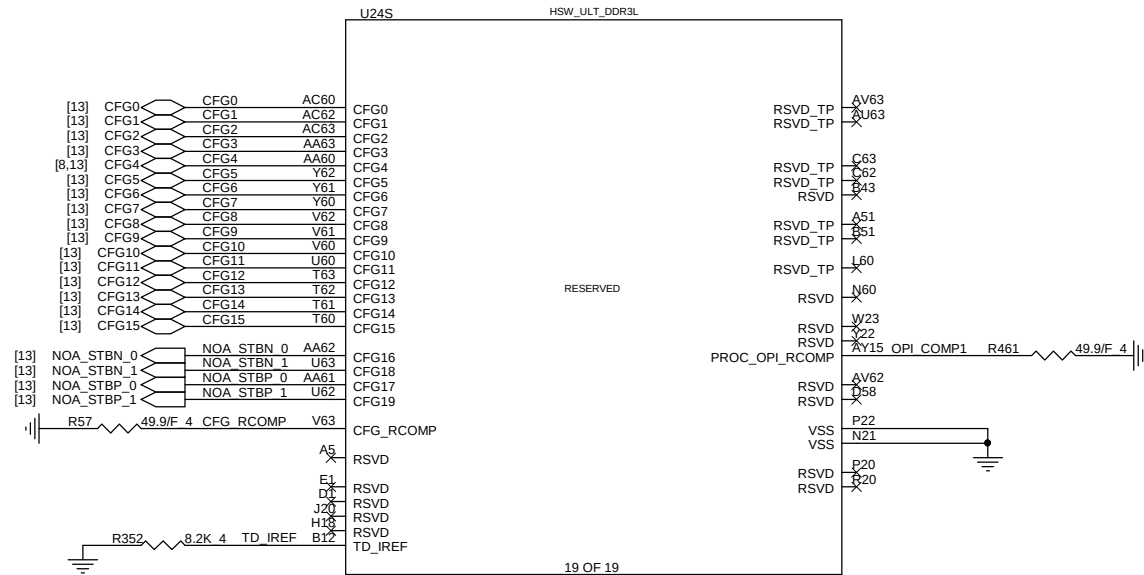
PROJECT : ZHN

Haswell 4/5 (POWER)

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Haswell ULT (CFG, RSVD)

06



Processor Strapping

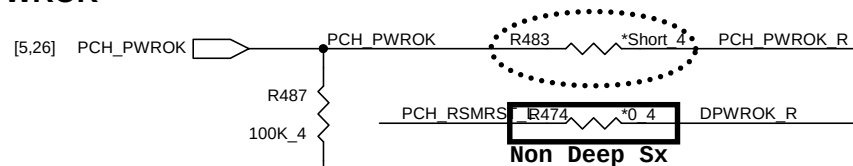
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R417 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R423 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K 4



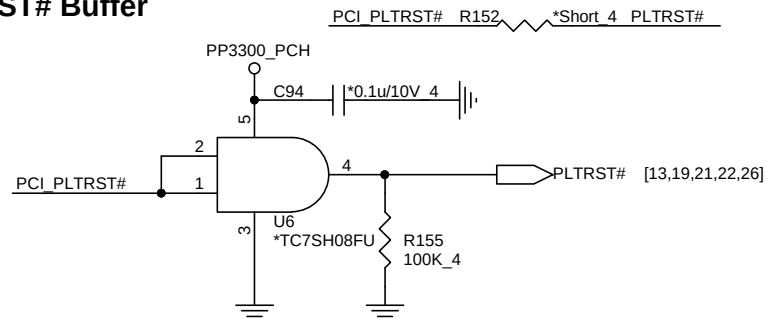
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3B
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07



4/22 modify, default is bypass PLTRST#

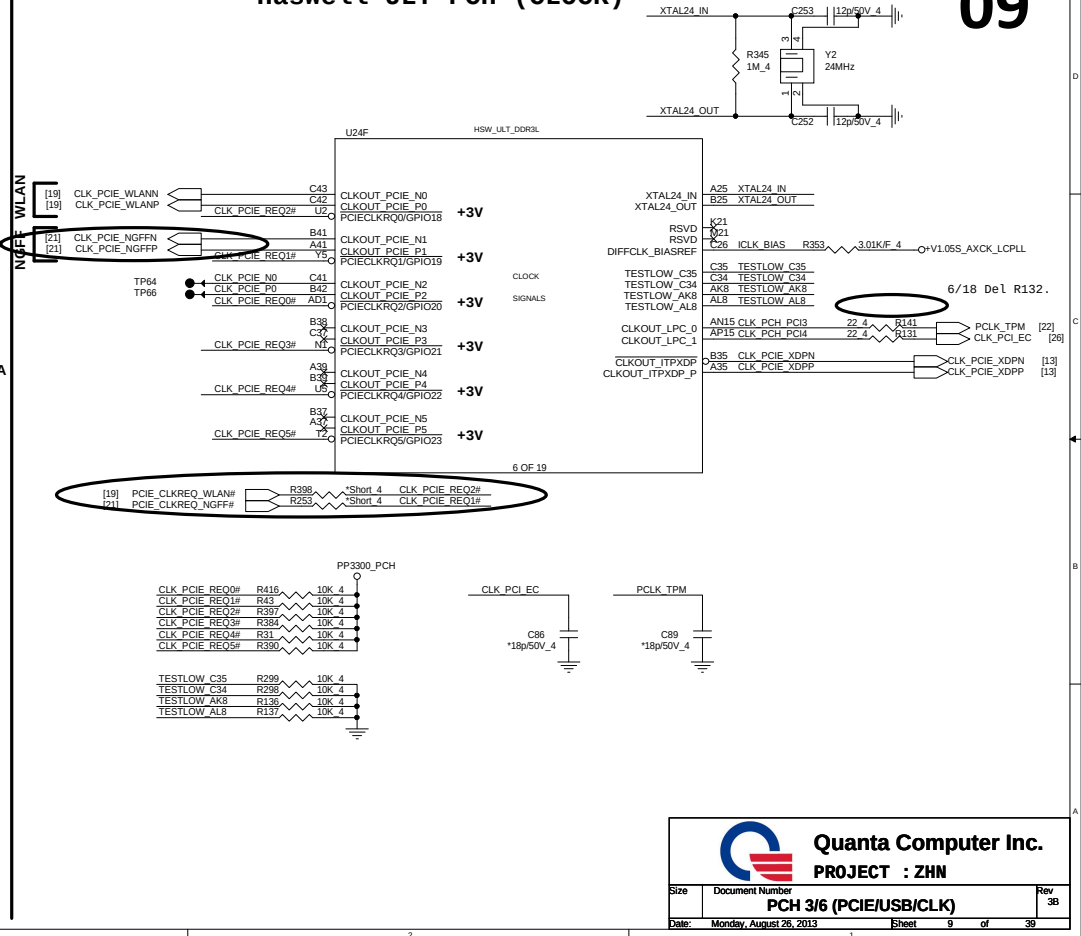


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Size	Document Number PCH 1/6 (PM)	Rev 3B
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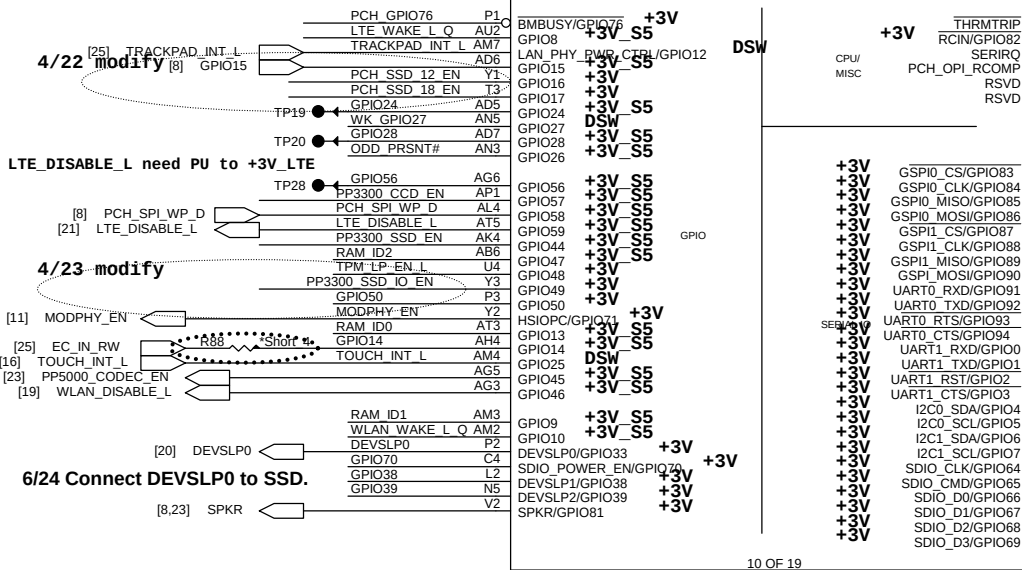
7/2 C278,C286 change to CH0150JB06.

09



Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U24J HSW_ULI_DDR3L



4/23 modify, those 3 power enable pin are PD 100K already

strapping

4/23 modify, follow Intel suggestion to un-stuff for unused GPIO

TRACKPAD

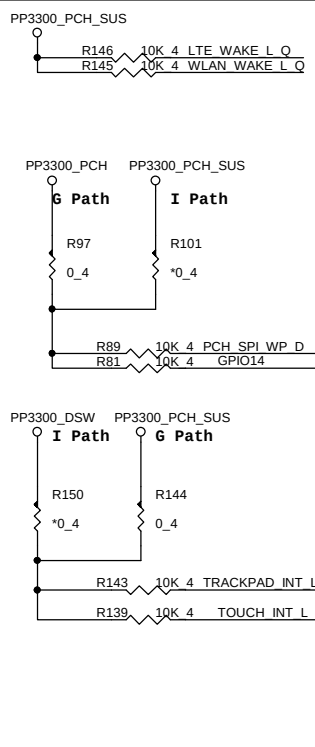
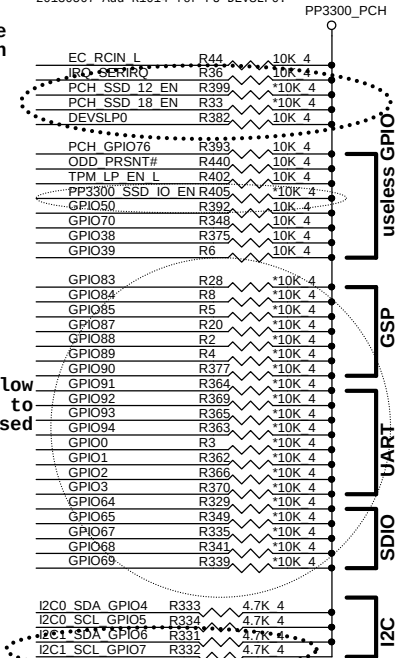
TOUCHSCREEN / ALS

strapping

PCH GPIO PU/PD

10

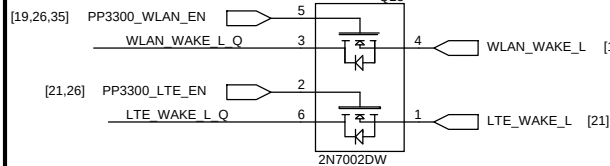
20130507 Add R1014 for PU DEVSLP0.



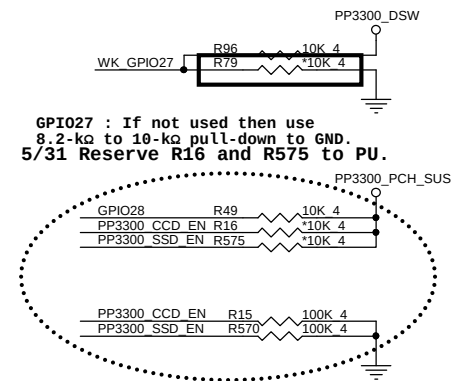
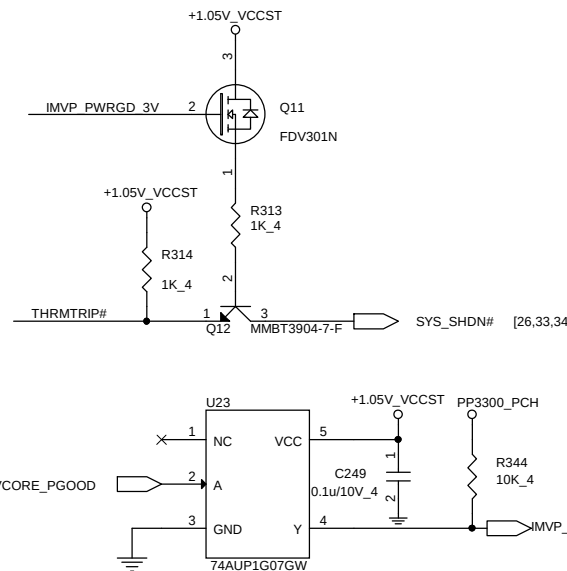
RAM ID

4/22 modify

Vender	RAM_ID			Q PN	Mfr. PN	Freq.
	ID2	ID1	ID0			
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHZ
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ
Elpida(4G)	0	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHZ
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHZ
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ
Elpida(2G)	1	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHZ



CPU thermal trip

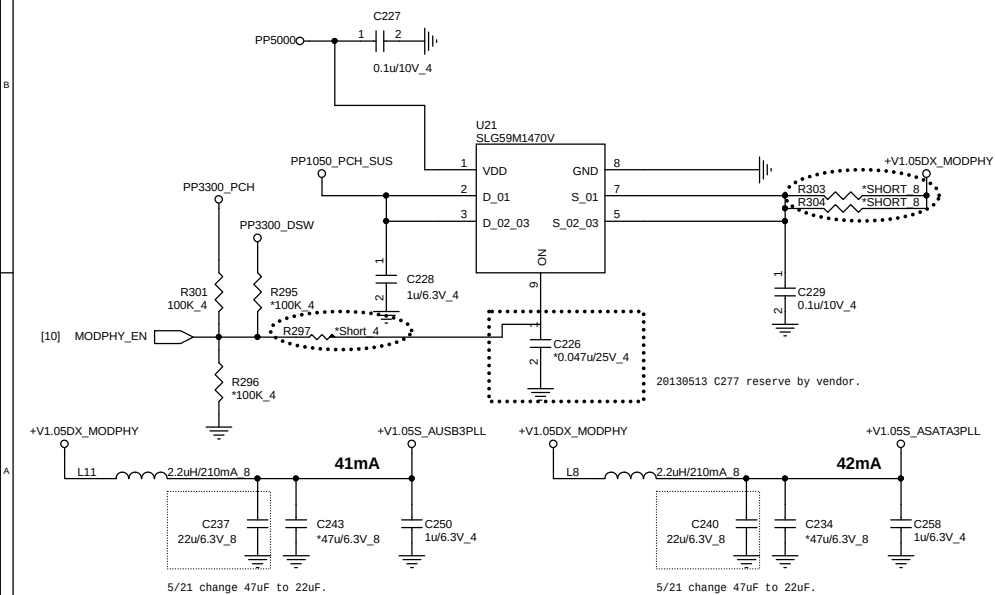


GPIO107 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND. 5/31 Reserve R16 and R575 to PU.

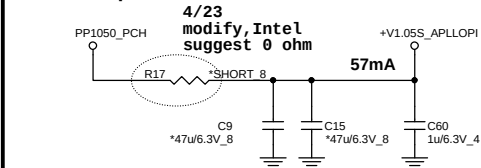
Haswell ULT PCH (Power)

0412 MOW-WW15 a 0.47uF cap between VccDSW3_3 and DcpSusByp is required if the 1.9A inrush current requirement cannot meet

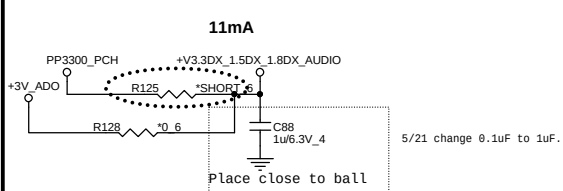
PCH VCCHSIO Power



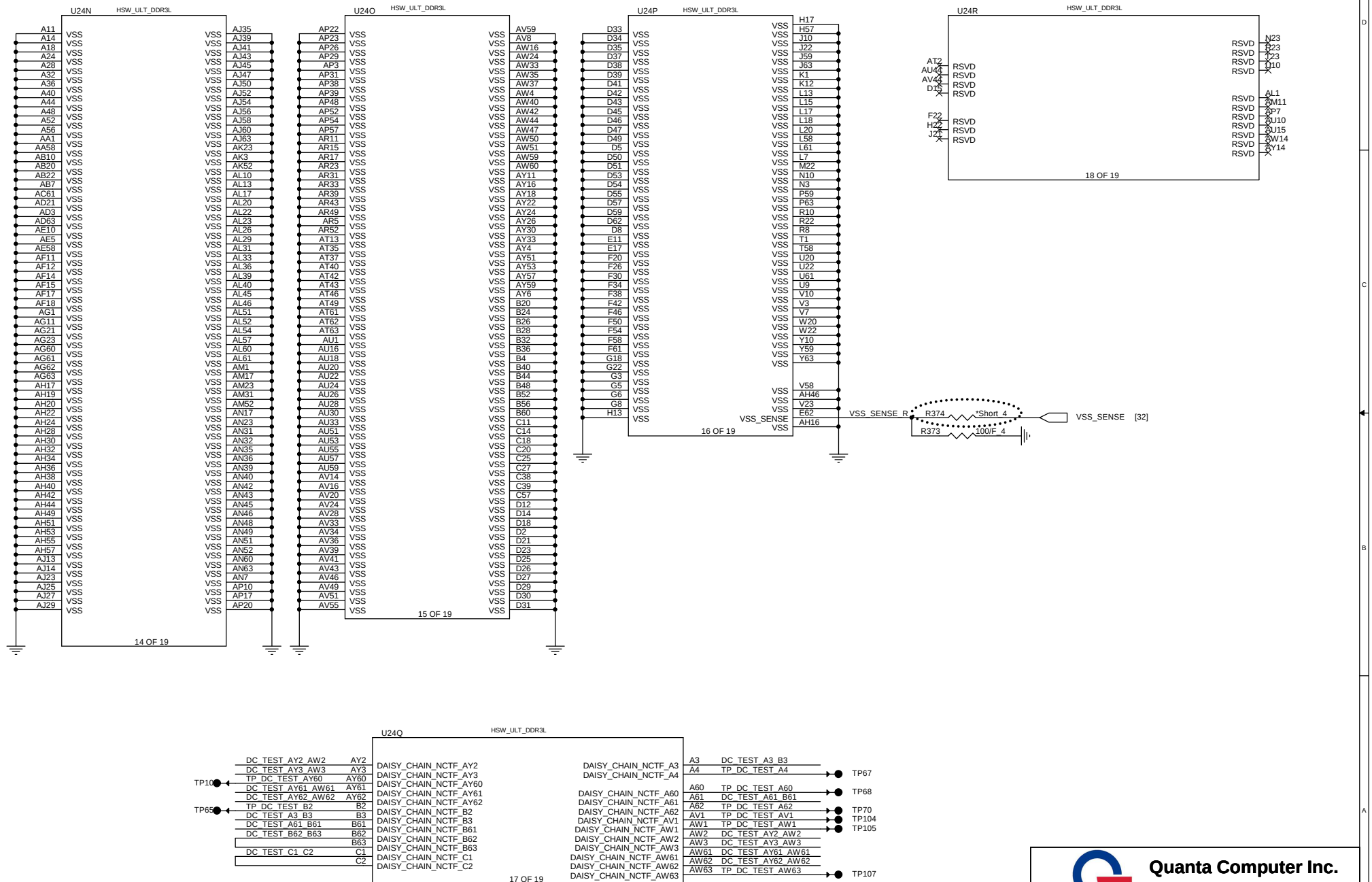
VCCAPLL power

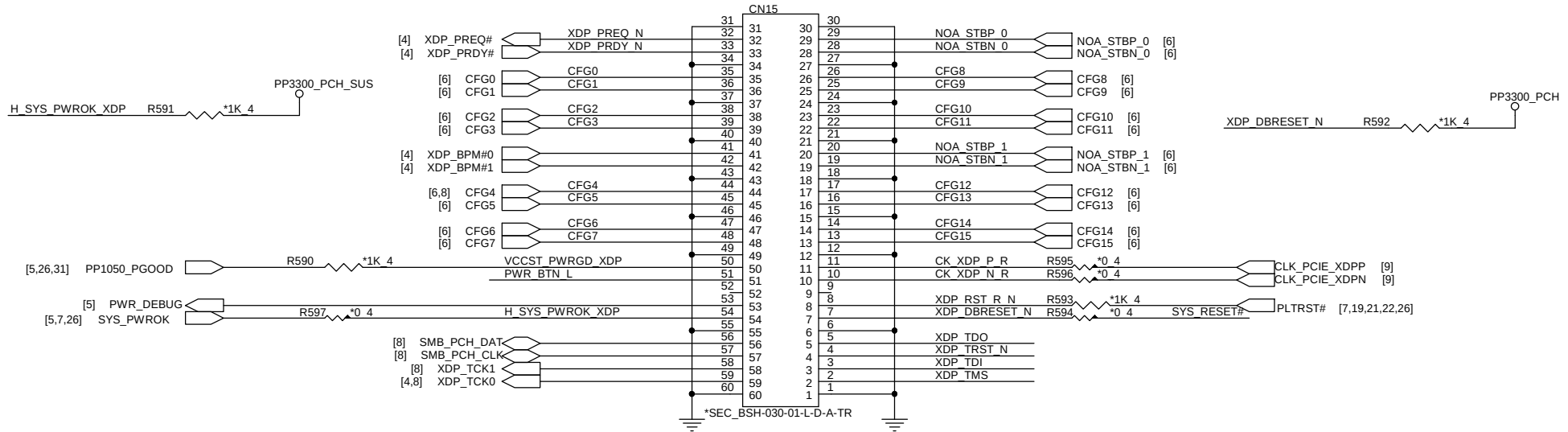


PCH HDA Power	
0	0.000000
1	0.000000
2	0.000000
3	0.000000
4	0.000000
5	0.000000
6	0.000000
7	0.000000
8	0.000000
9	0.000000
10	0.000000
11	0.000000
12	0.000000
13	0.000000
14	0.000000
15	0.000000
16	0.000000
17	0.000000
18	0.000000
19	0.000000
20	0.000000
21	0.000000
22	0.000000
23	0.000000
24	0.000000
25	0.000000
26	0.000000
27	0.000000
28	0.000000
29	0.000000
30	0.000000
31	0.000000
32	0.000000
33	0.000000
34	0.000000
35	0.000000
36	0.000000
37	0.000000
38	0.000000
39	0.000000
40	0.000000
41	0.000000
42	0.000000
43	0.000000
44	0.000000
45	0.000000
46	0.000000
47	0.000000
48	0.000000
49	0.000000
50	0.000000
51	0.000000
52	0.000000
53	0.000000
54	0.000000
55	0.000000
56	0.000000
57	0.000000
58	0.000000
59	0.000000
60	0.000000
61	0.000000
62	0.000000
63	0.000000
64	0.000000
65	0.000000
66	0.000000
67	0.000000
68	0.000000
69	0.000000
70	0.000000
71	0.000000
72	0.000000
73	0.000000
74	0.000000
75	0.000000
76	0.000000
77	0.000000
78	0.000000
79	0.000000
80	0.000000
81	0.000000
82	0.000000
83	0.000000
84	0.000000
85	0.000000
86	0.000000
87	0.000000
88	0.000000
89	0.000000
90	0.000000
91	0.000000
92	0.000000
93	0.000000
94	0.000000
95	0.000000
96	0.000000
97	0.000000
98	0.000000
99	0.000000

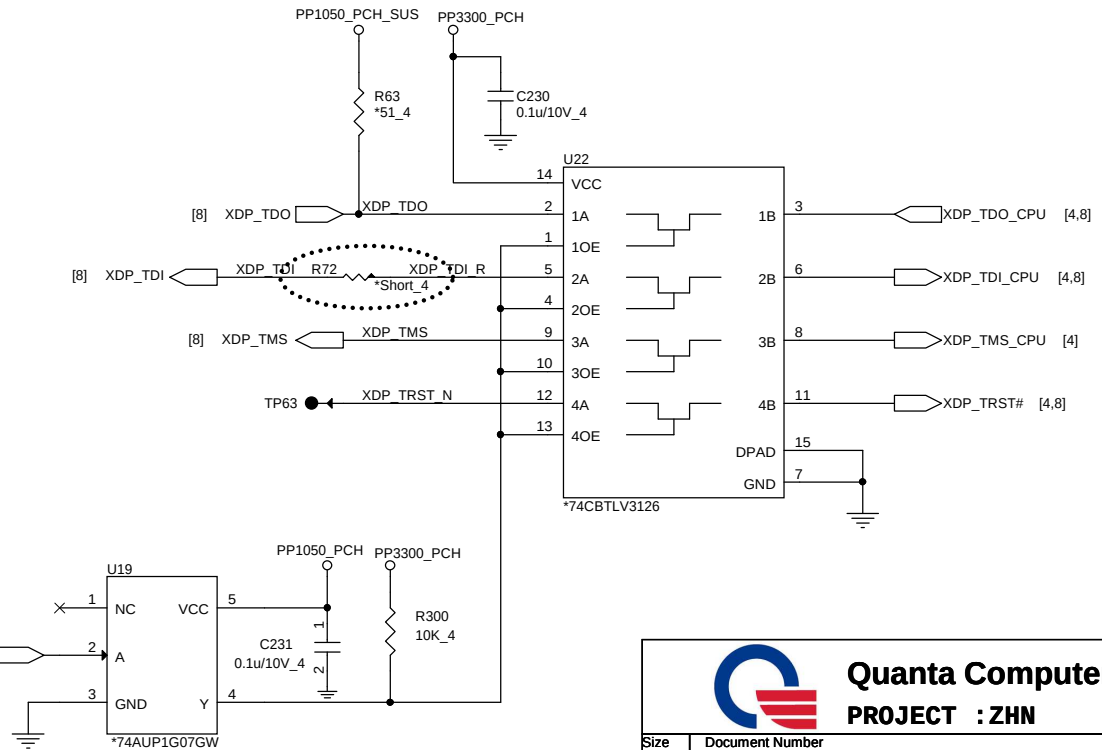
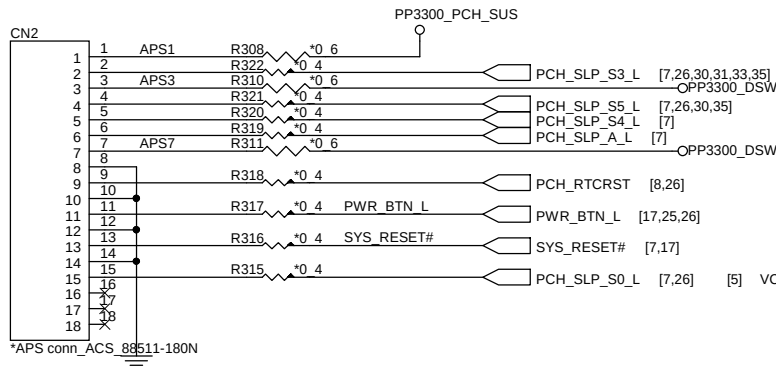


Haswell ULT (GND)





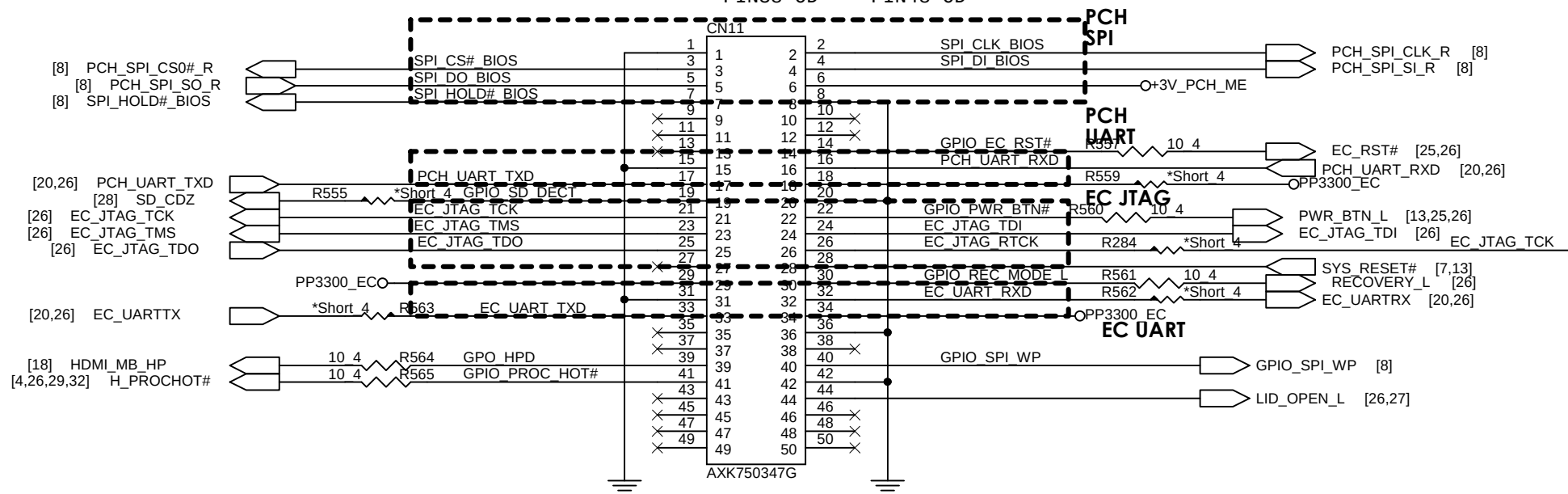
APS





Debug Port(DBG)

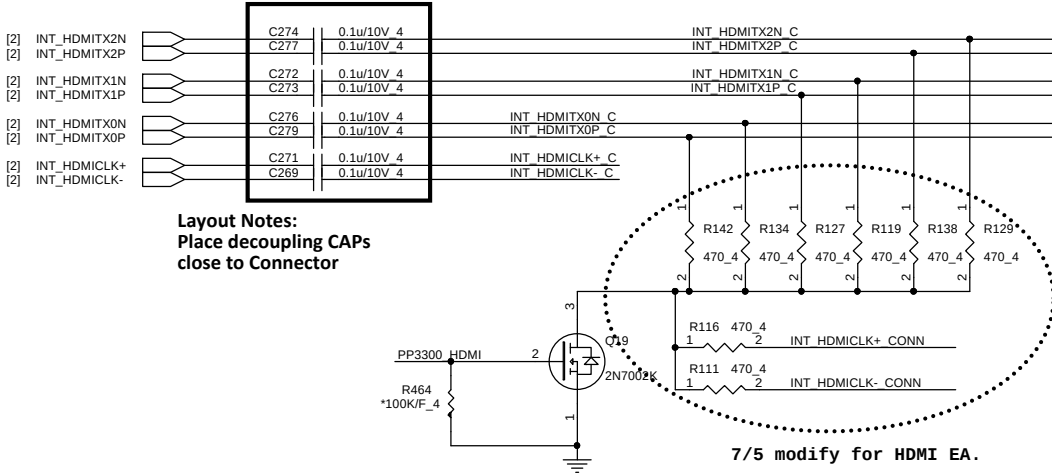
PIN7 OD PIN39 OD PIN49 OD
 PIN14 OD PIN41 OD PIN50 OD
 PIN19 OD PIN43 OD
 PIN22 OD PIN44 OD
 PIN28 OD PIN45 OD
 PIN30 OD PIN46 OD
 PIN37 OD PIN47 OD
 PIN38 OD PIN48 OD



Quanta Computer Inc.
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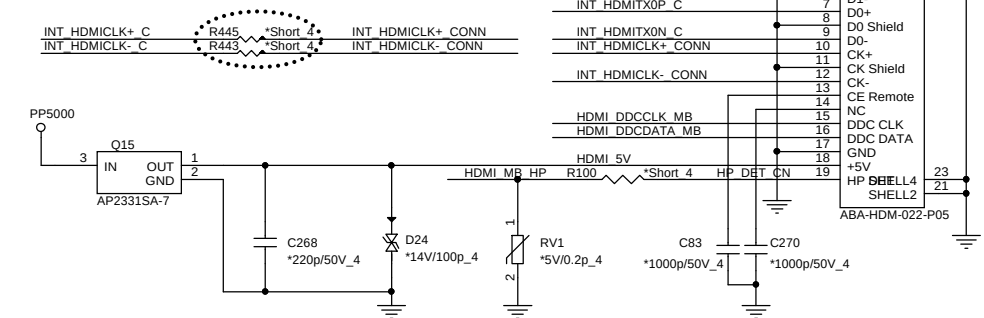
HDMI Cost Reduced level shift (HDM)



HDMI connector (HDM)

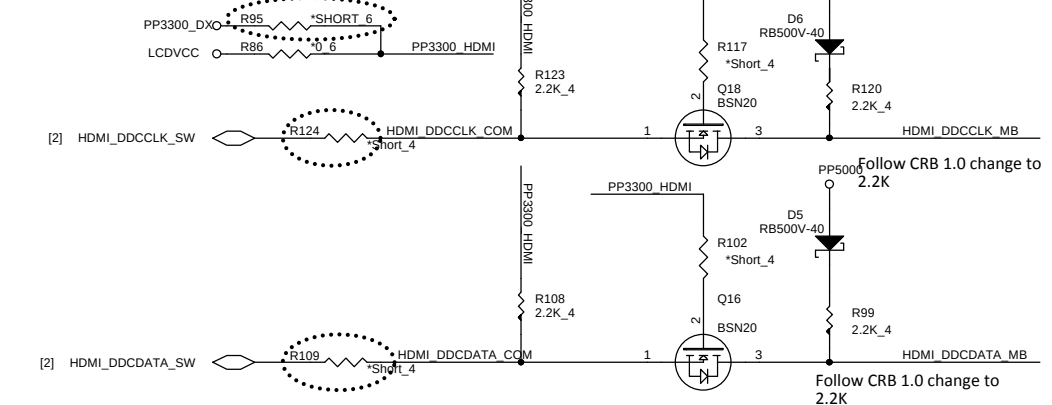
DFHS19FR079
new footprint not ready

8/21 Del L13 and R443, R445
change to shortpad.

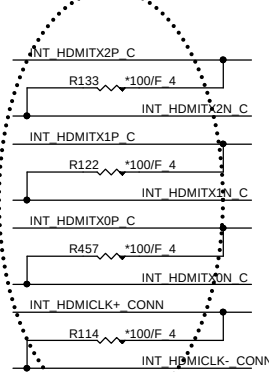


18

HDMI DDC (HDM)

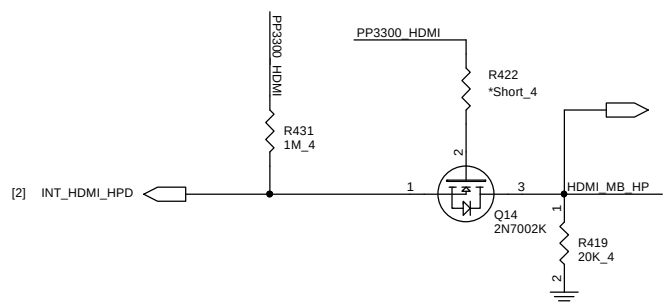


EMI (EMC)



4/22 modify for layout
7/5 unstuff by HDMI EA.

HDMI-detect (HDM)

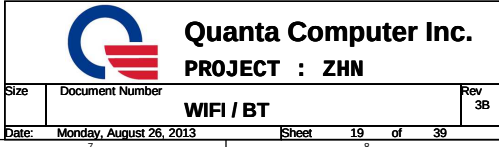




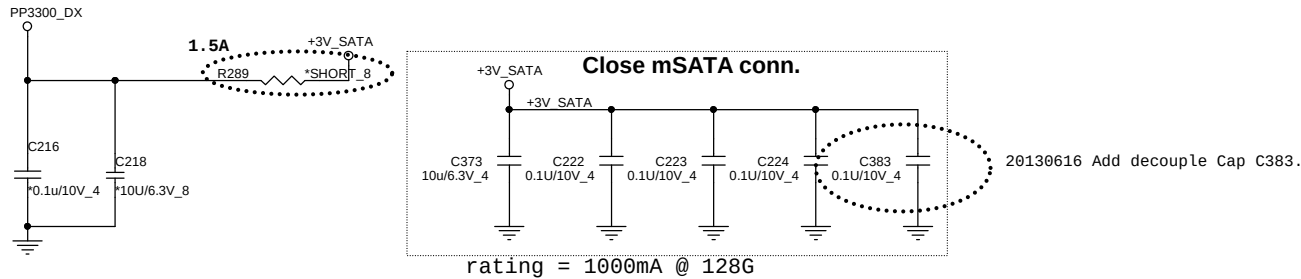
Quanta Computer Inc.
PROJECT : ZHN
HDMI

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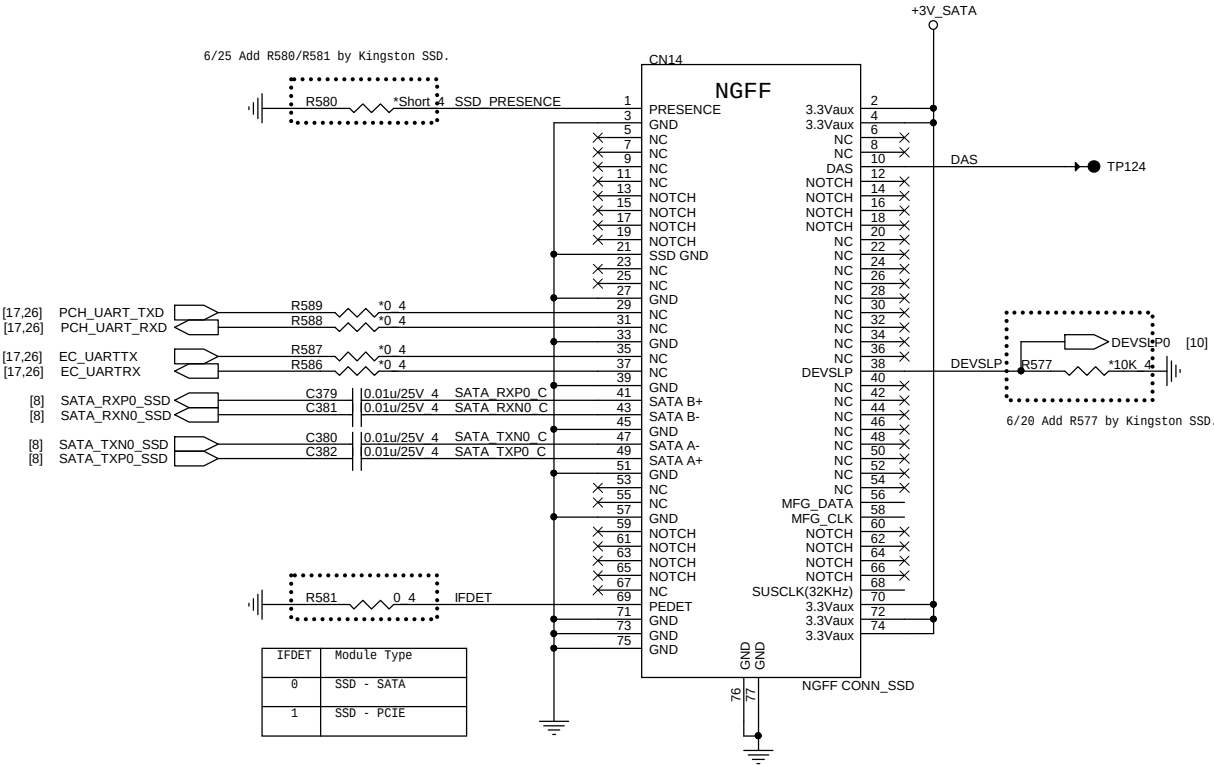
19



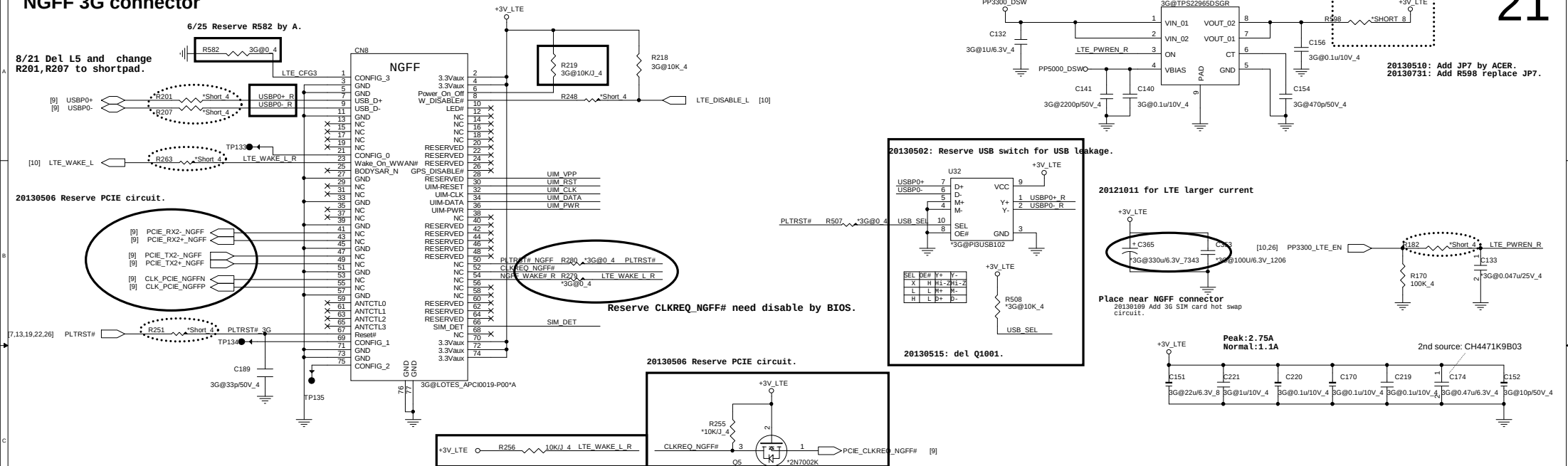
NGFF SSD connector.
San Disk SSD Card.



20130521 Page20 Change CN14 to NGFF type.



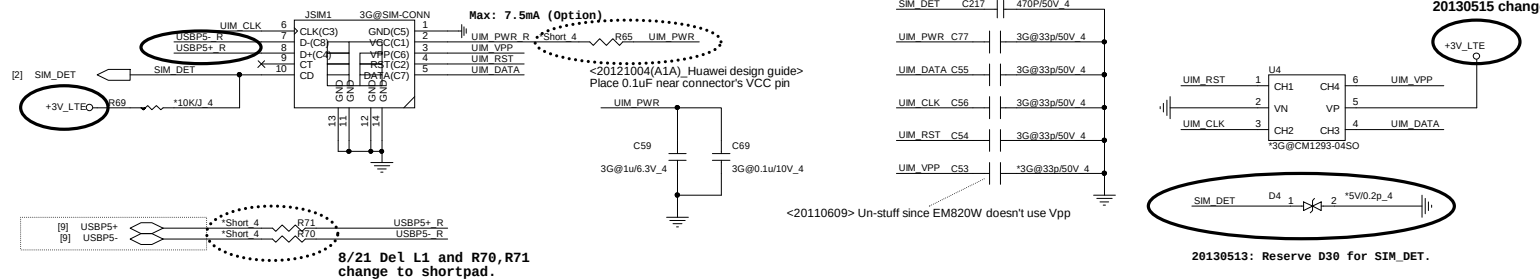
NGFF 3G connector



MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.

5/14 Add R65



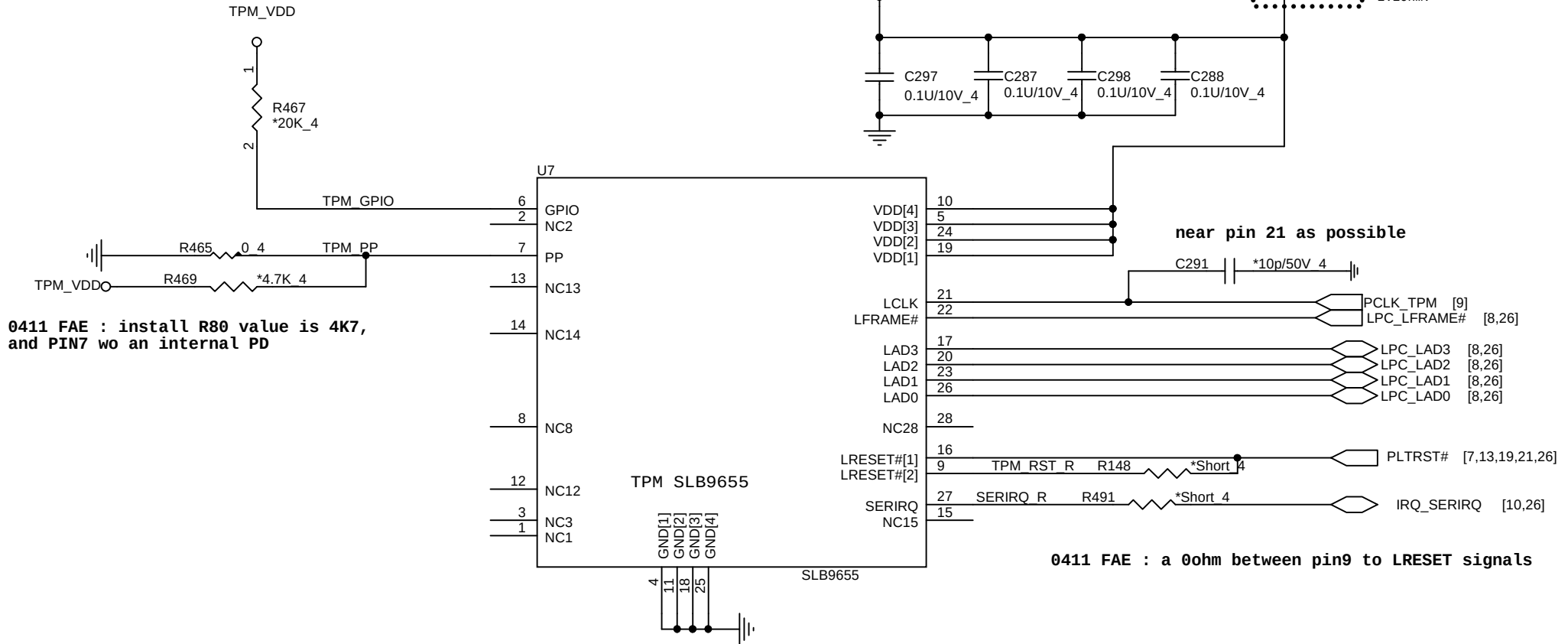
20130513: Reserve D30 for SIM_DET.

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NGGF/ SIM conn		
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TPM (TPM)

22

4 x100nF (place close to device VDD/GND pins)



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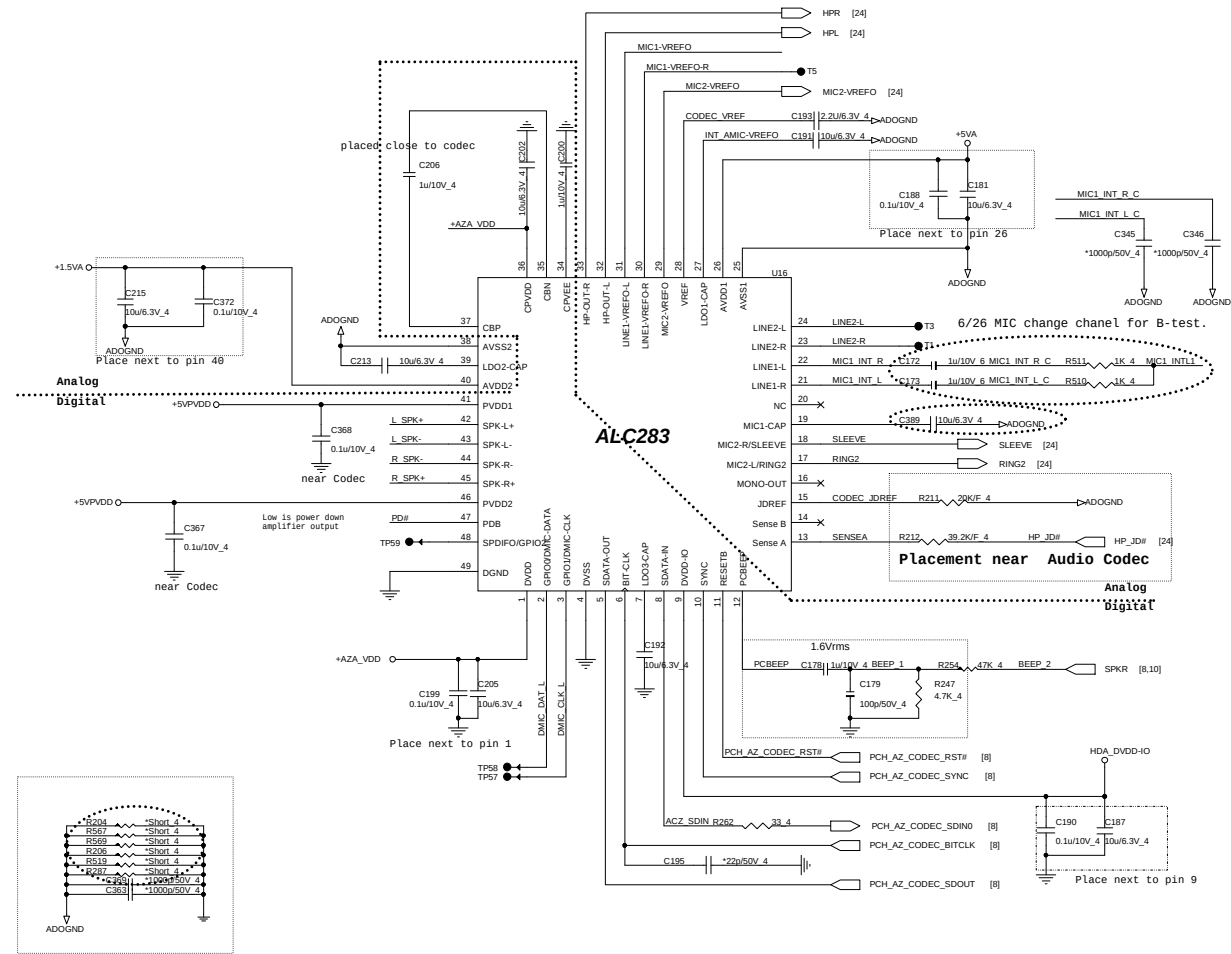
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	TPM SLB9655 / LED	3B

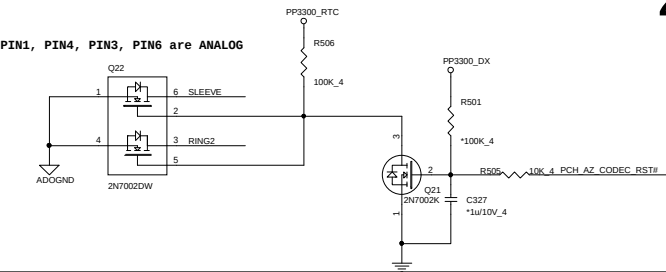
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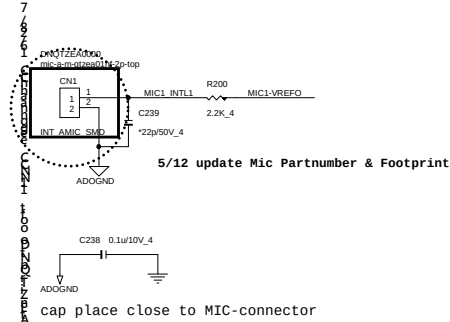
Codec(ADO)



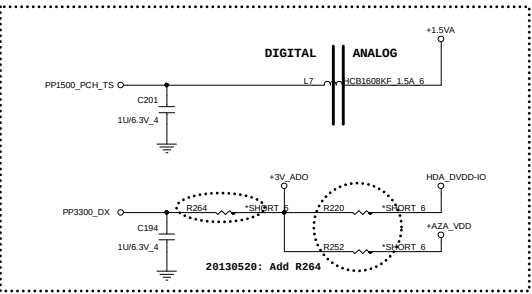
Grounding circuit(ADO)



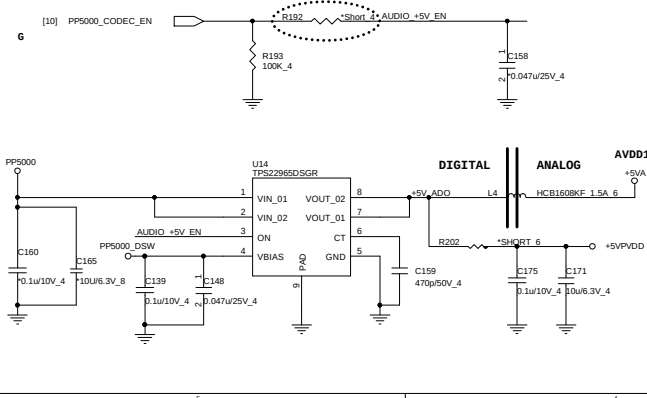
INT MIC array



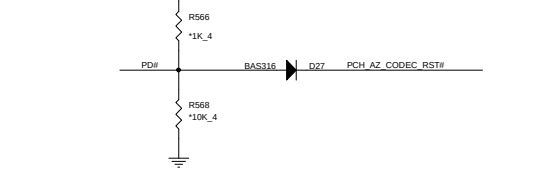
Codec PWR 3V/1.5V(ADO)



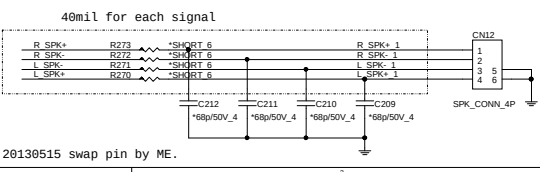
Codec PWR 5V(ADO)



Mute(ADO)



Internal Speaker

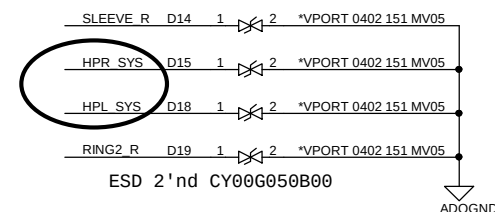


24

9) Change L16, L21 from 00000 to 0ohm by SMT.

The diagram shows a circuit with the following components and connections:

- MIC2-VREFO**: A pin header connection at the top.
- R214** and **R283**: Both are $2.2K_4$ resistors connected in parallel between **MIC2-VREFO** and **RING2**.
- RING2**: A pin header connection on the left.
- SLEEVE**: A pin header connection at the bottom.
- L21** and **L16**: Inductors highlighted with dashed circles. They are labeled with **0 4**, indicating they are to be replaced with 0-ohm resistors.

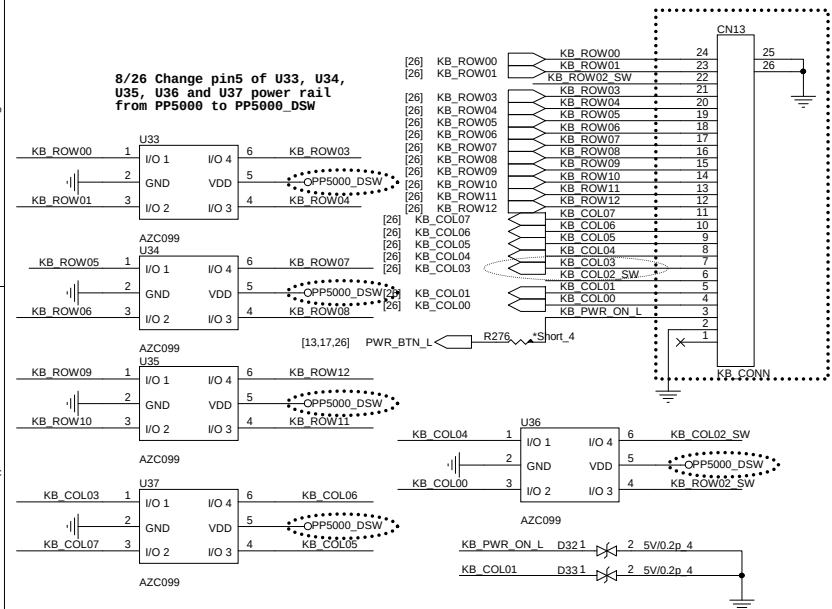


ESD 2'nd CY00G050B00

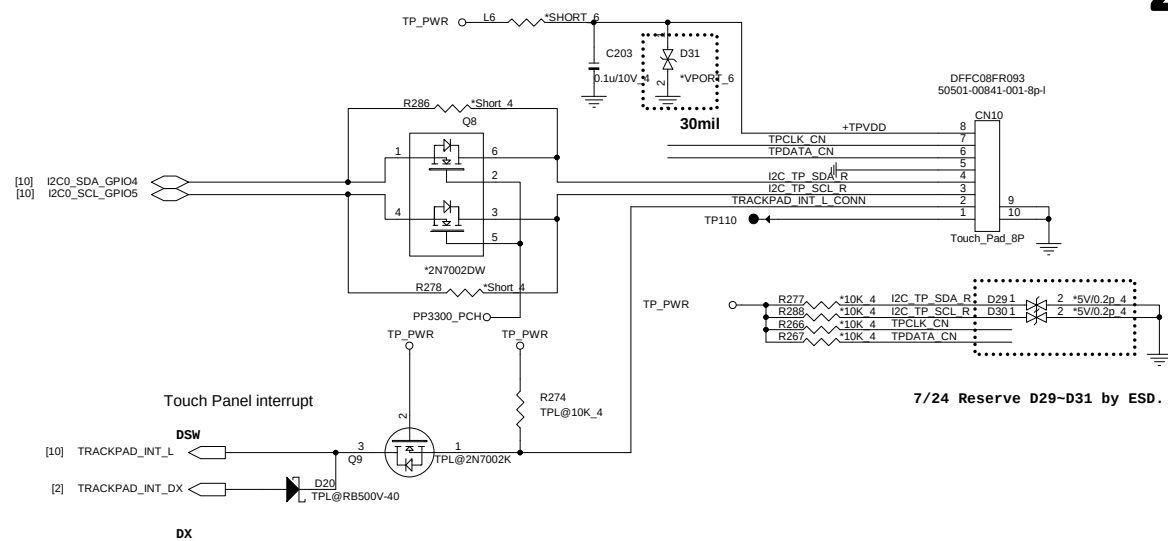
 Quanta Computer Inc. PROJECT : ZHN		Rev
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Audio Headset SW		
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K/B (KBC)

8/22 DFFC24FR098
footprint 88502-2401-24P-L-SMT



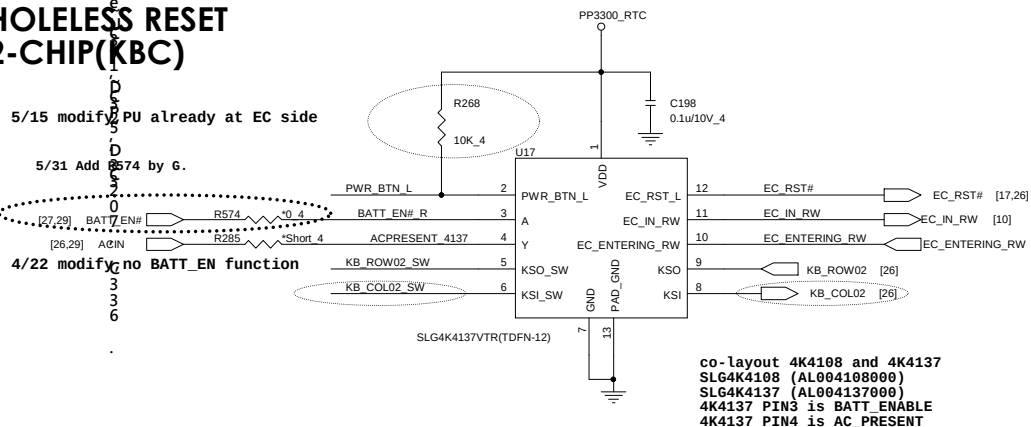
TOUCHPAD BOARD CONN (TPD)

HOLELESS RESET
2-CHIP(KBC)

5/15 modify CPU already at EC side

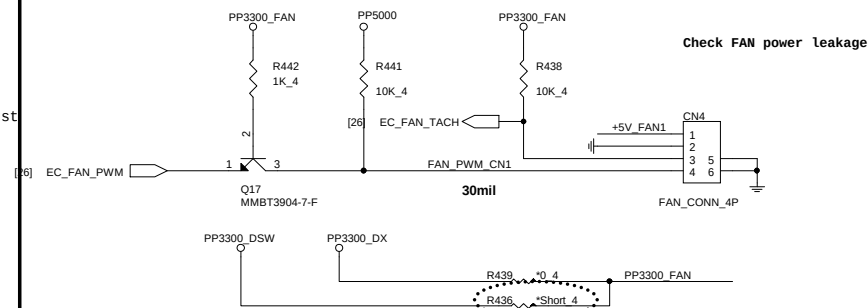
5/31 Add R574 by 6.

4/22 modify no BATT_EN function



CPU FAN1 (THM)

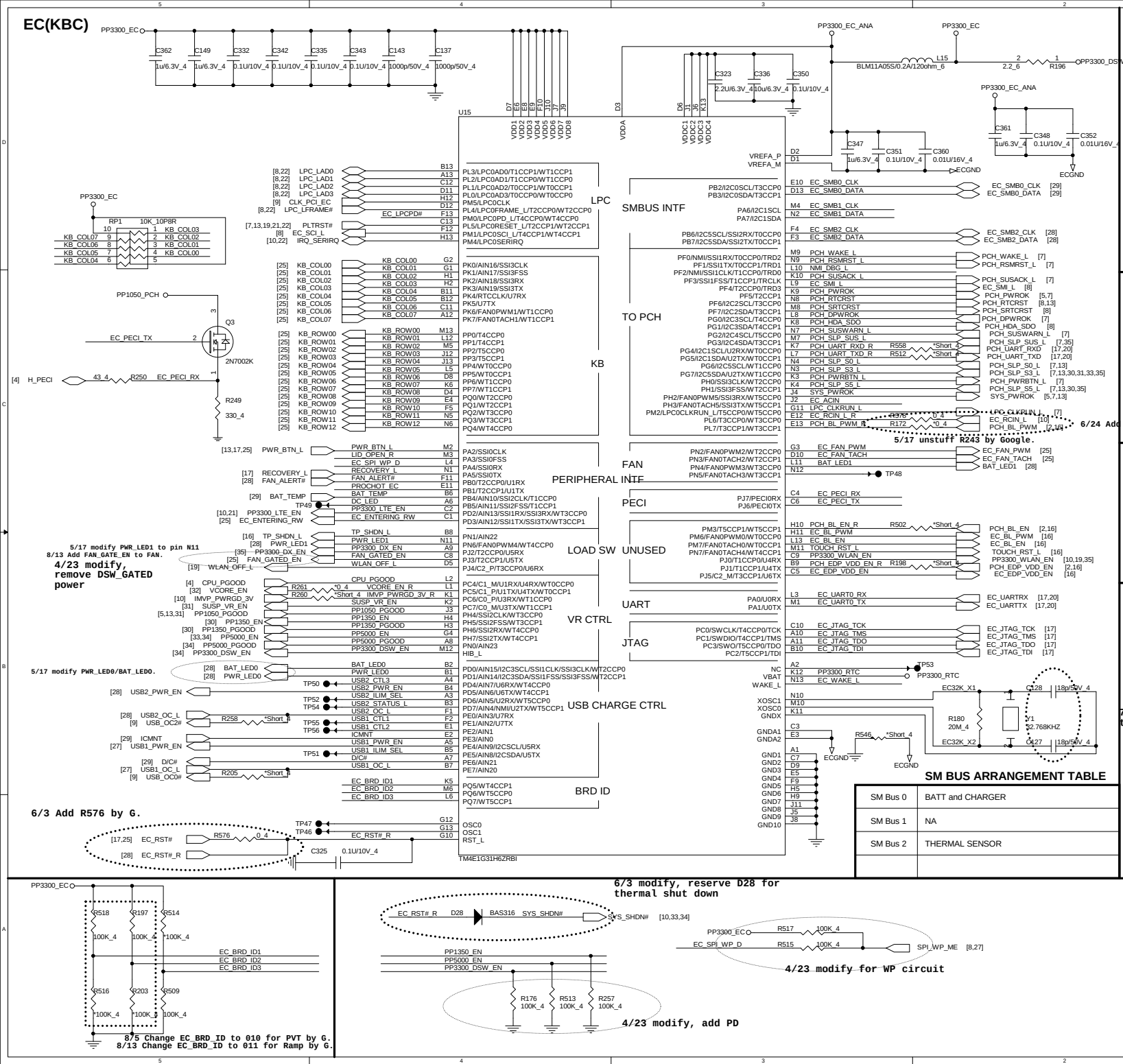
Check pin define 0321
footprint 88266-040xx-xxx-4p-1



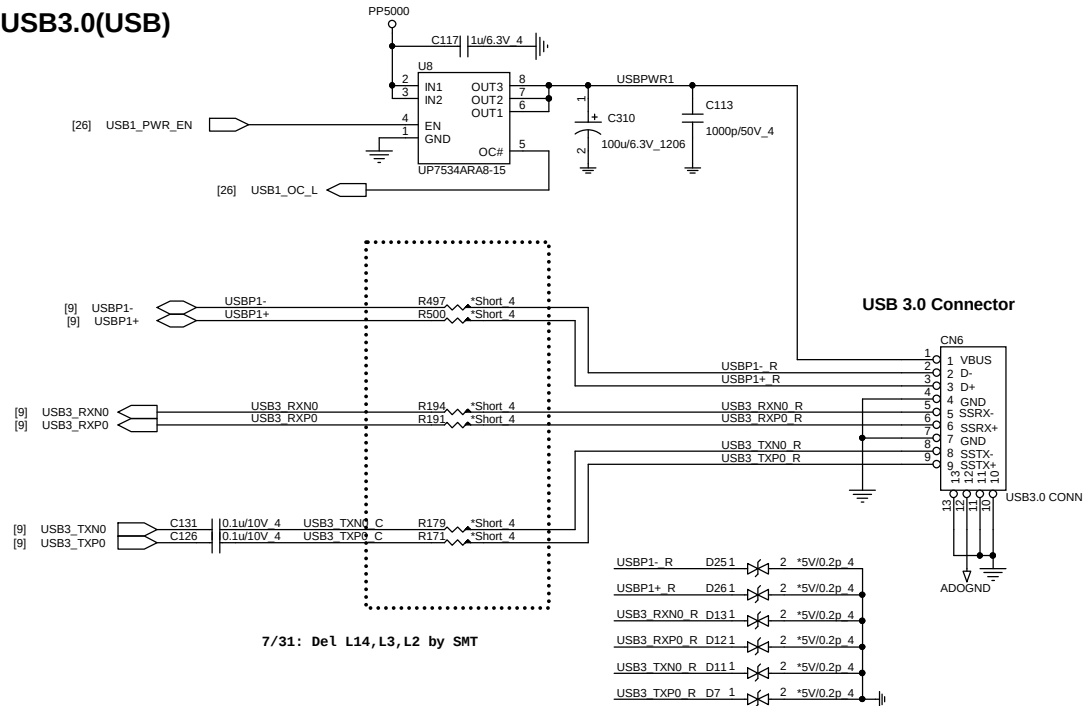
Quanta Computer Inc.
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	KB/TP/FAN/HW Reset	38
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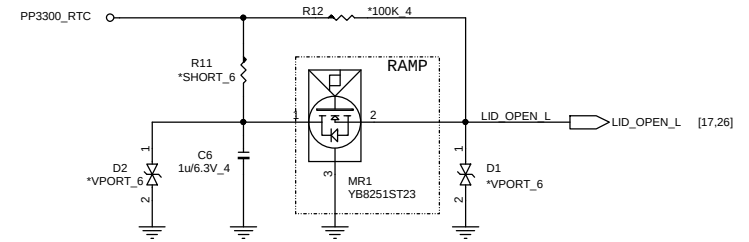
EC(KBC)



USB3.0(USB)

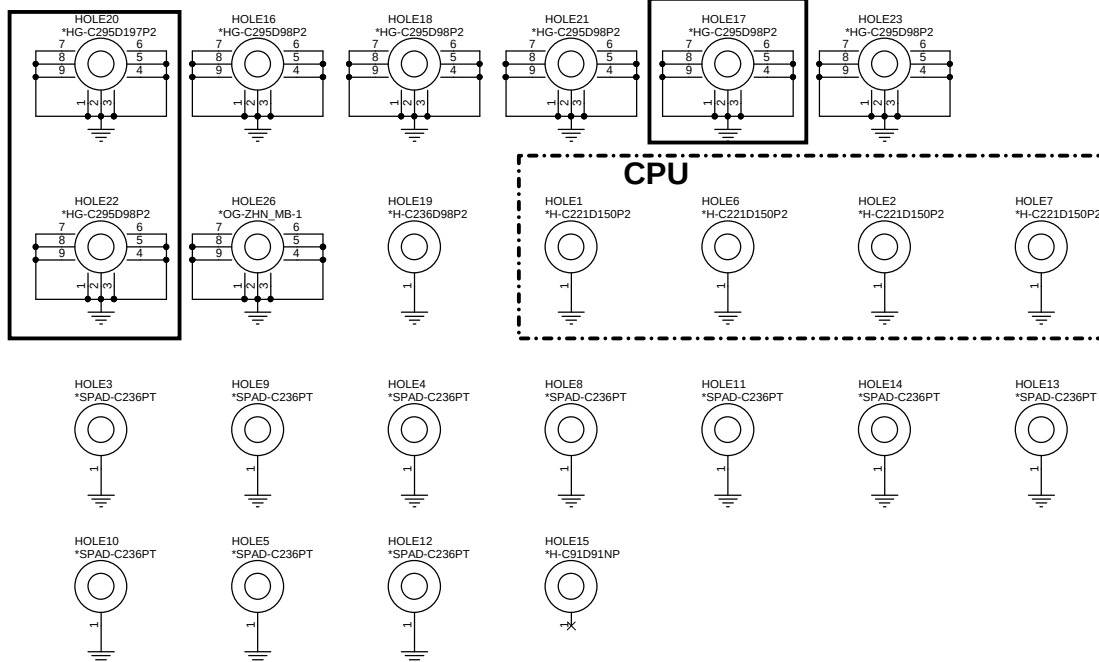


Lid Switch (HSR)

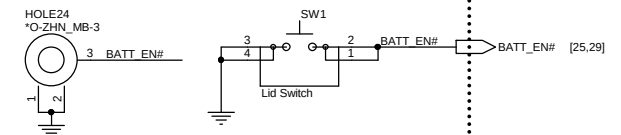


HOLE(OTH)

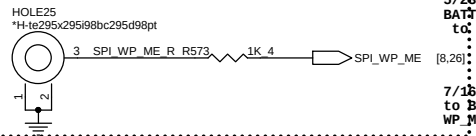
6/26 change footprint by ME.



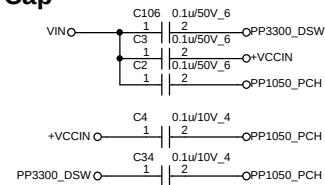
BATT Enable short pad



ROM WP#



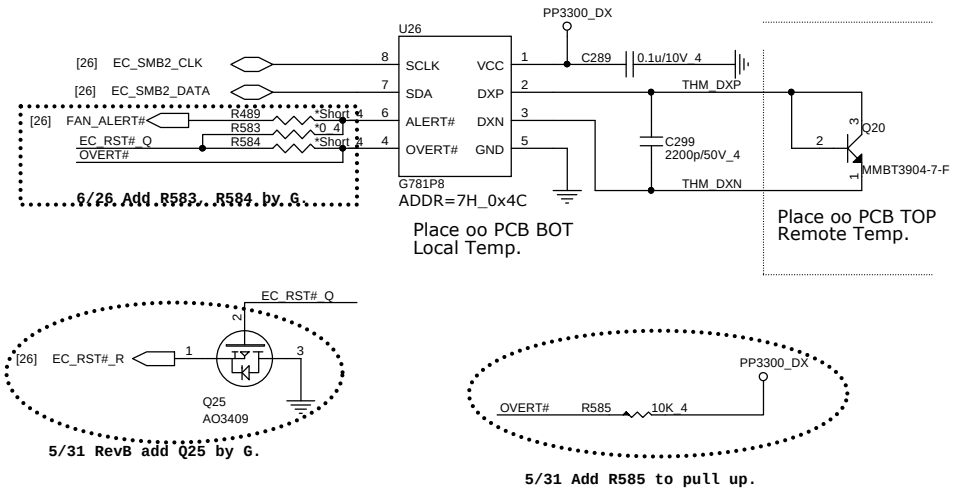
EMI Cap



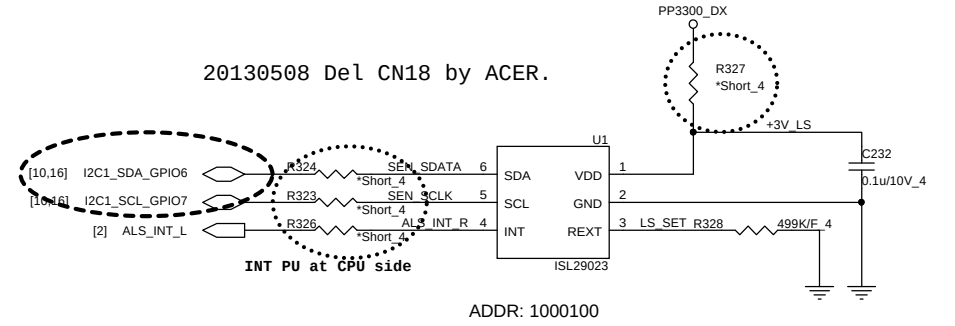
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	USB3/Hole	3B
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Thermal Sensor(THM)

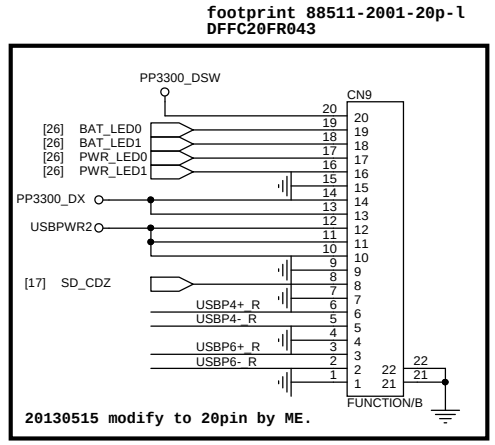
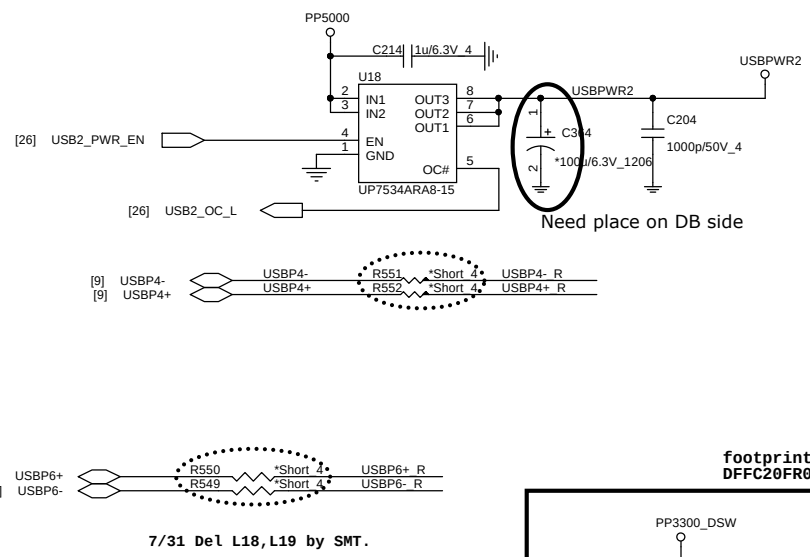


Light sensor & TP (SER)



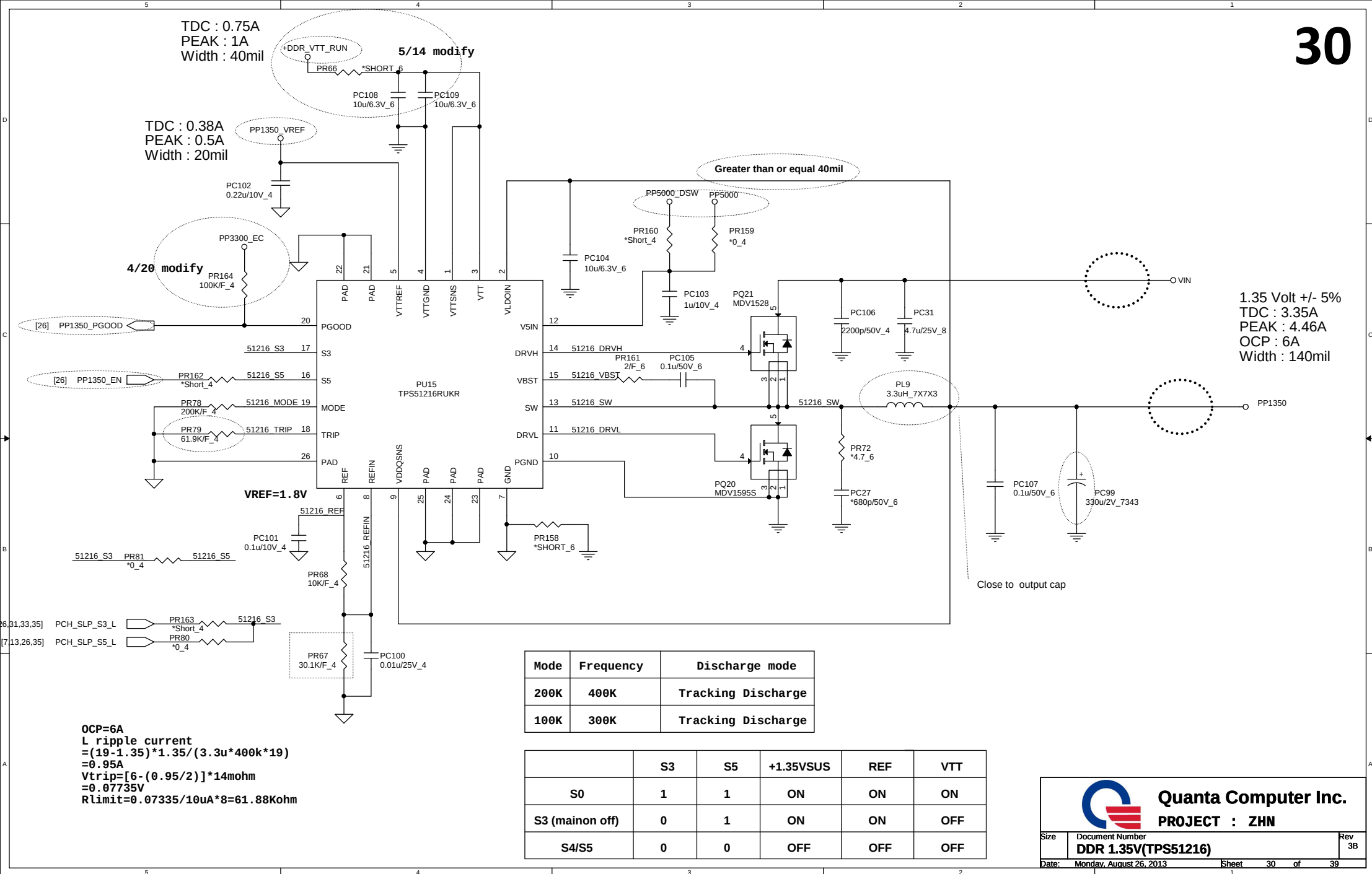
FUNCTION DB

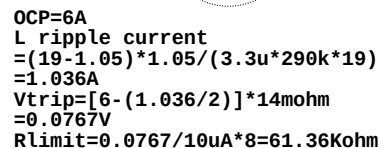
HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2



Quanta Computer Inc.
PROJECT : ZHN

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	DB/ALS/Thermal sensor	3B
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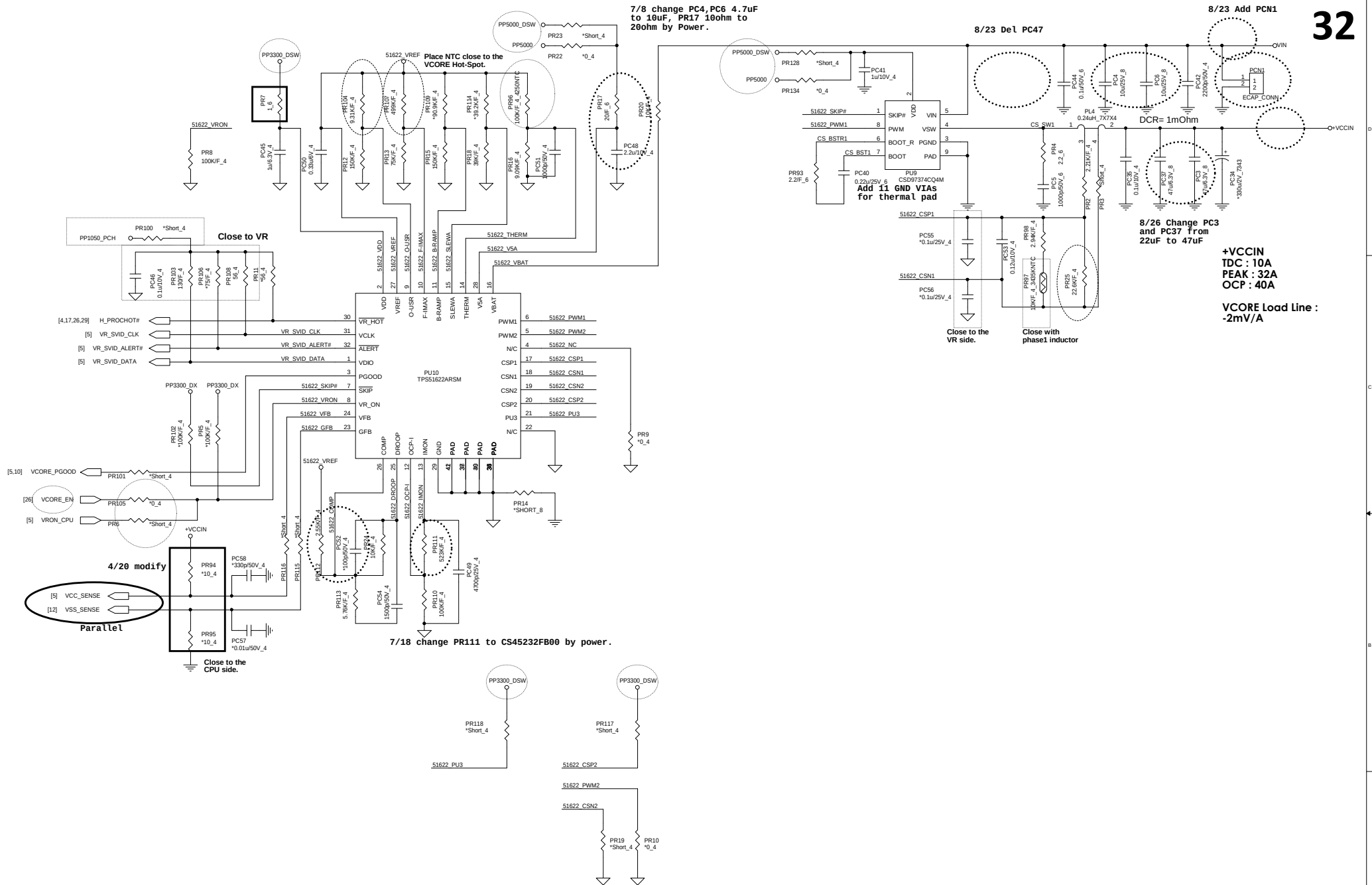


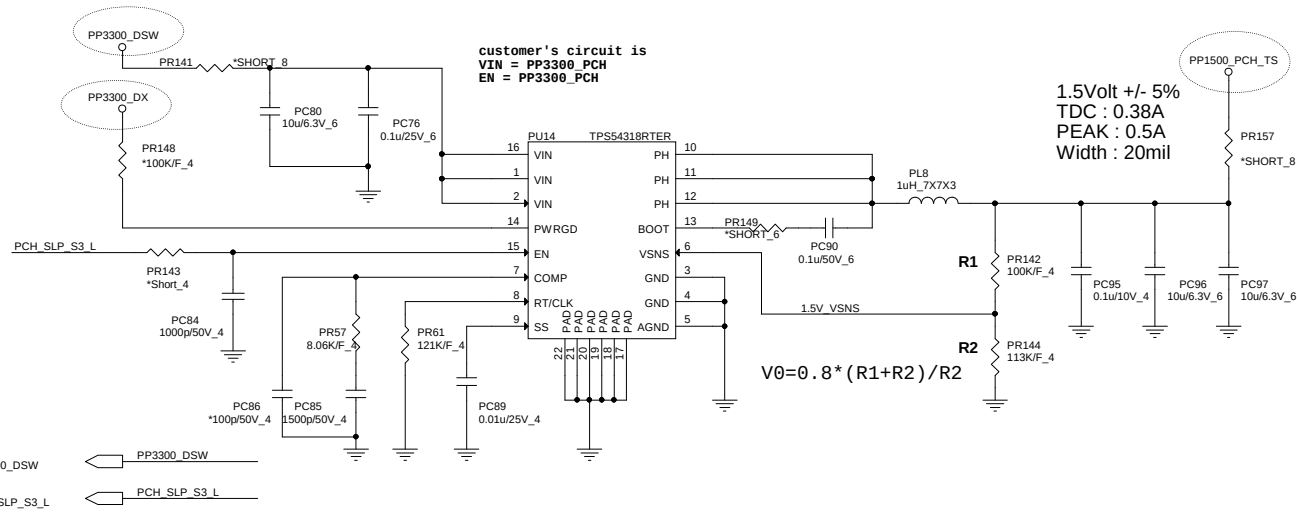


← PCH SLP S3 L



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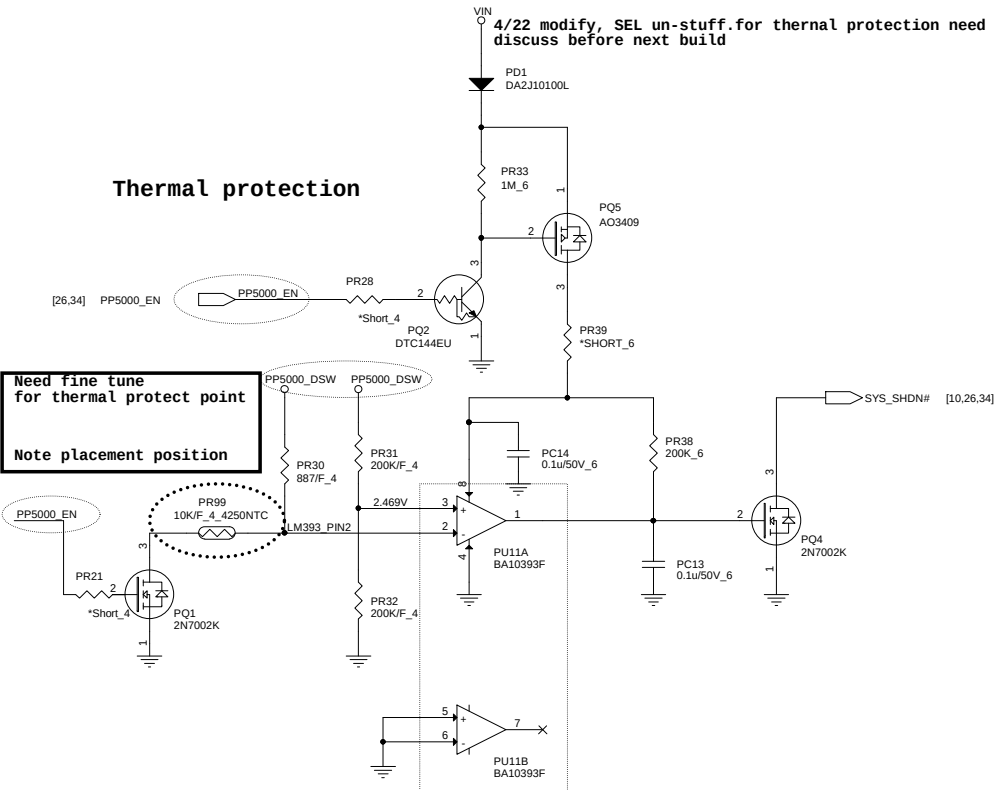


[21,25,26,27,28,32,34,35] PP3300_DSW
[7,13,26,30,31,35] PCH_SLP_S3_L

4/22 modify, SEL un-stuff.for thermal protection need
discuss before next build

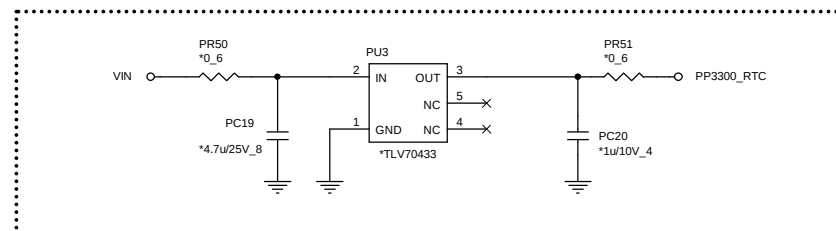
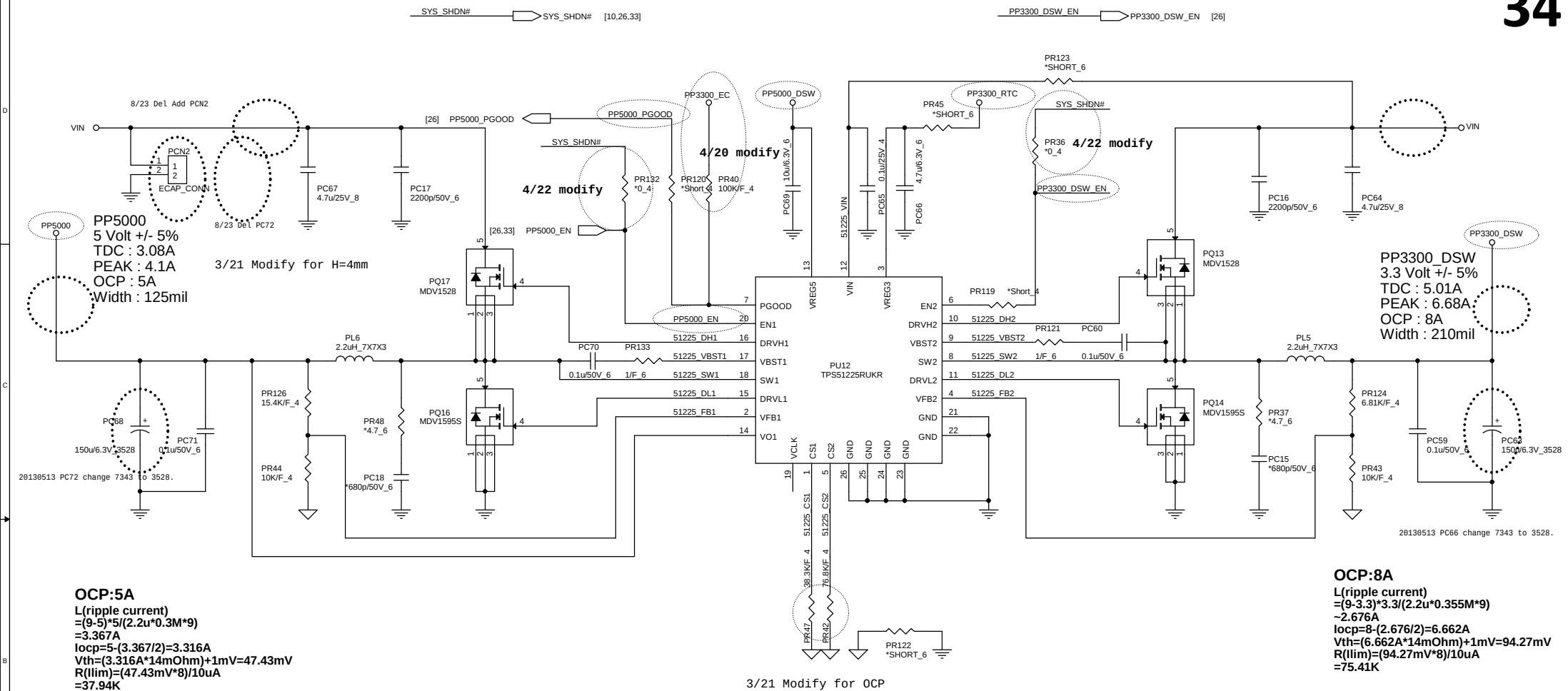
Thermal protection

Need fine tune
for thermal protect point
Note placement position

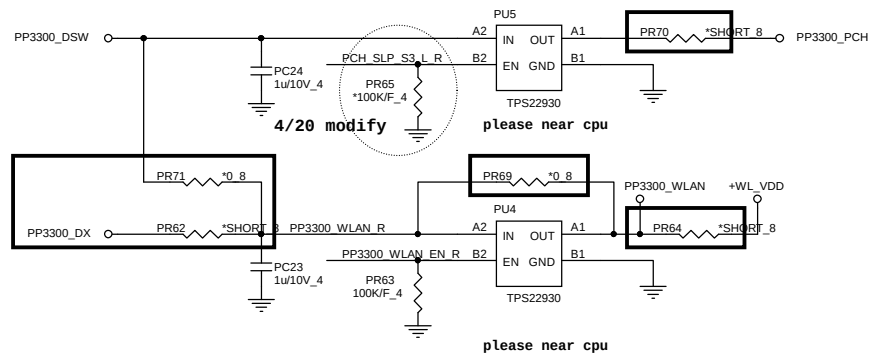
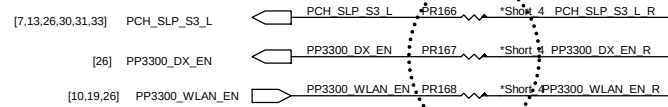


Quanta Computer Inc.
PROJECT : ZHN

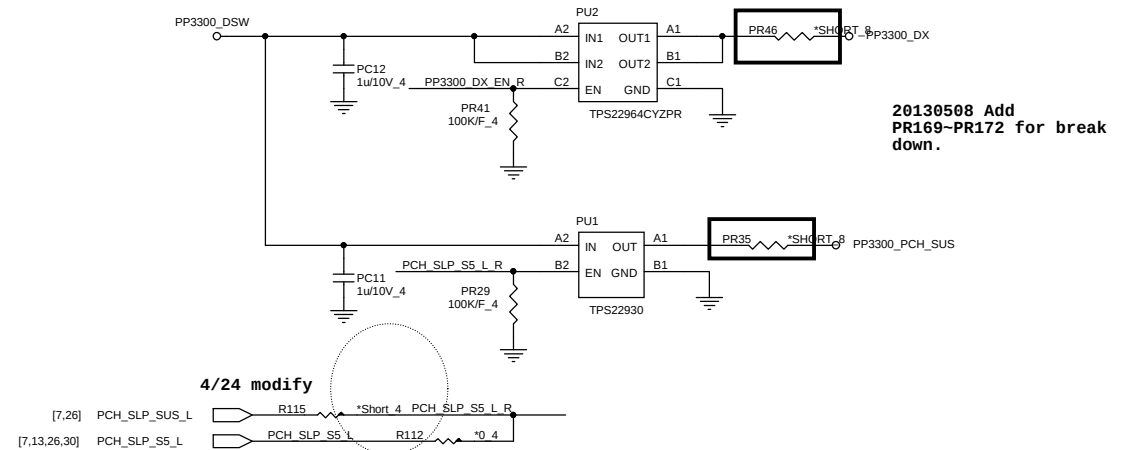
Size	Document Number	Rev
	+1.2V/+1.5V/+1.8V/Thermal protect	3B
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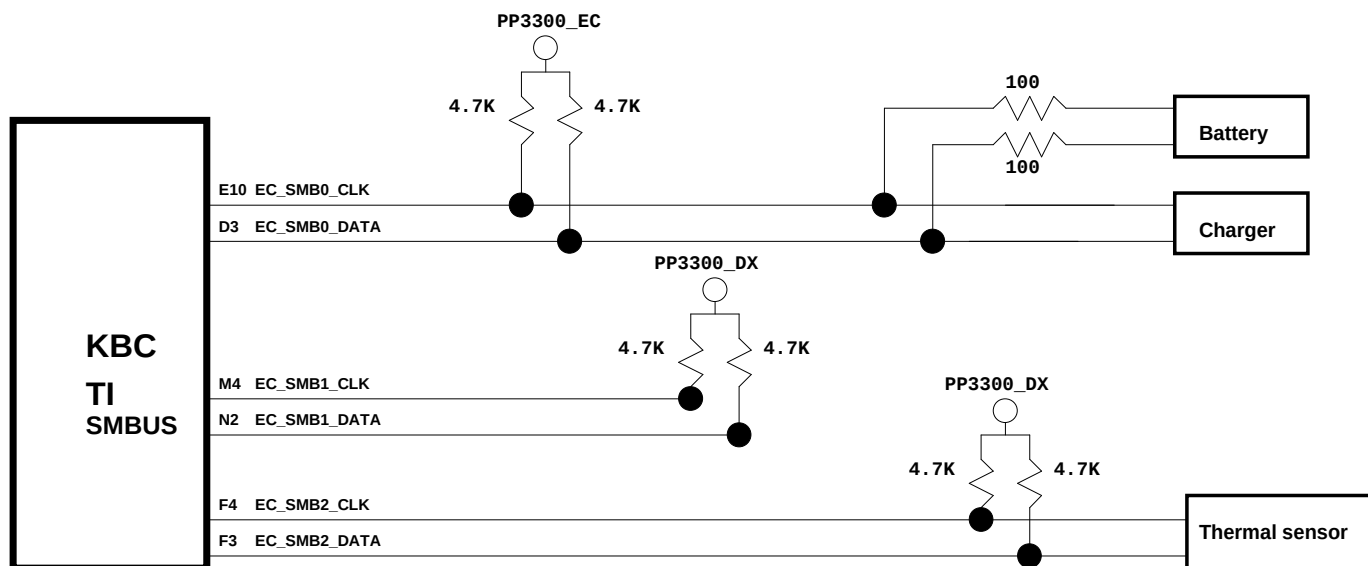
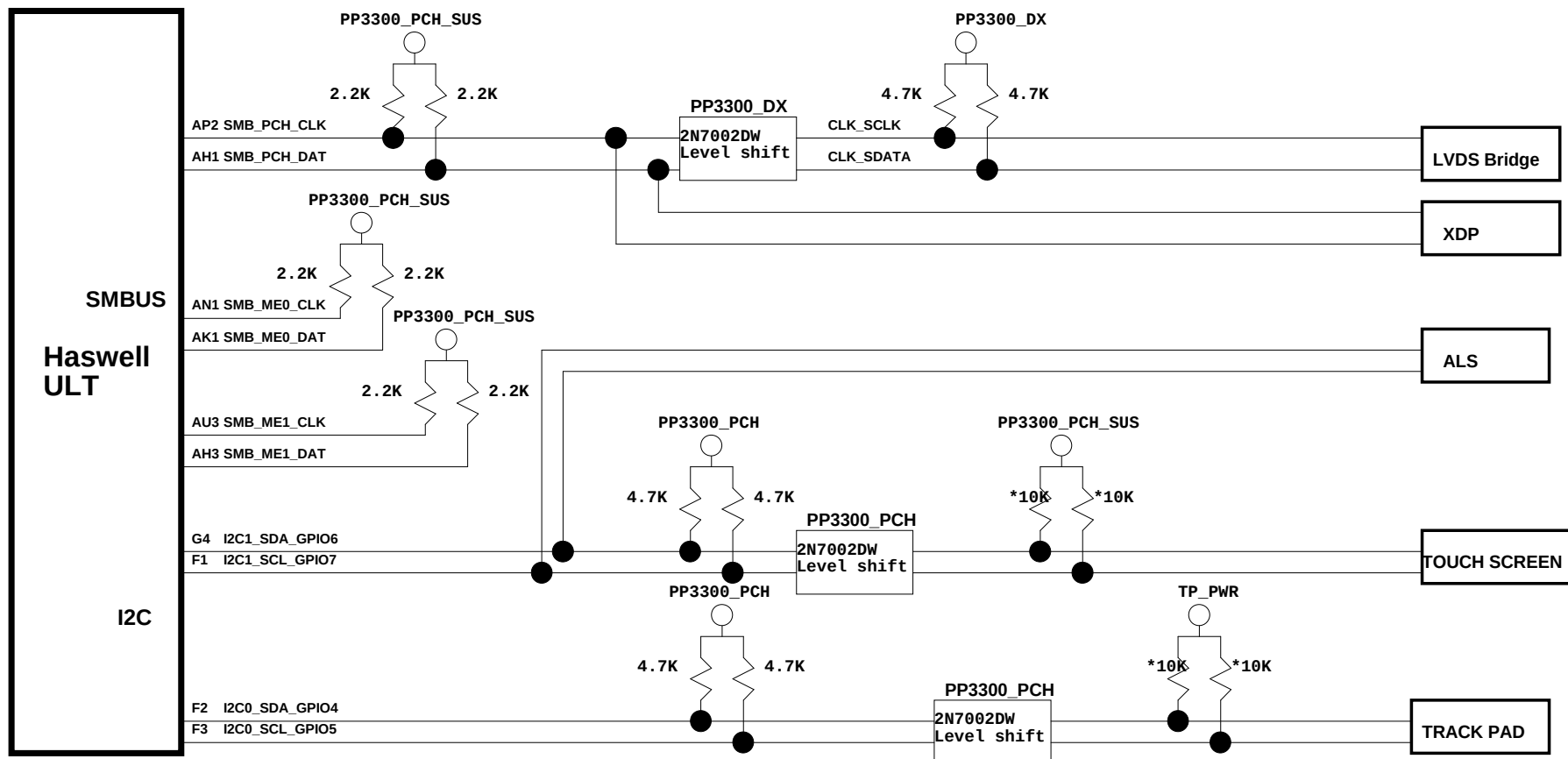


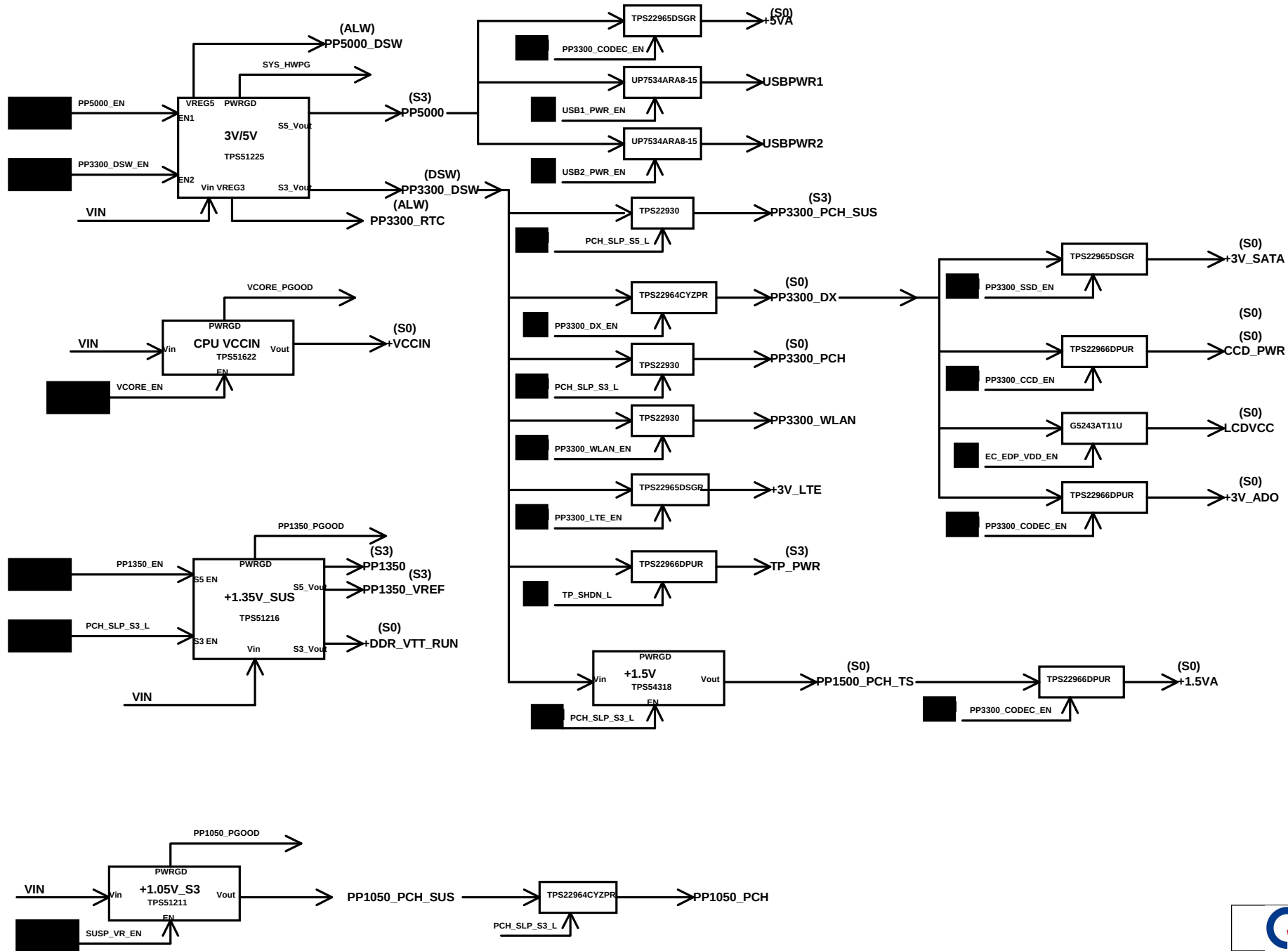
6/23 Add PR166~168 for debug.



20130517 Page35 Add PR174 & reserve PR175,PR176 to input pwr PU4 by ACER.







Model	Version	CHANGE LIST
Benneton	1A	2018062 Page21: Change net name USBPWR_R to USBPWR_R and USBPWR_R to USBPWR_R 2018062 Page21: Reserve USB switch USBR0, USBR1,R0B01 for USB Isolate. 2018062 Page31 Del +LVB_SSD,+LVN_SSD power circuit. 2018062 Page31 Del CN1 for XDP debug. 2018062 Page37 Del RVSDV_DP EEPROM Mode straping R163,R162,R176,R177. 2018062 Page38 Del DMIC: circuit DAU1,R421,R422,C135,C136. 2018062 Page39 Del DMIC & Auto switch by Cntrlg. 2018062 Page39 Add Cap C6410-C6413. 2018062 Page39 Change P11 and P12 Isotripair. 2018062 Page39 Add USMRP and CLK_P1,LPC with R1004. 2018062 Page21 Change AMIC(CN17) Isotripair to mic-ax224-sdb2ip. 2018062 Page21 Reserve PCIe Power to U50H pin45 connect to GND & change JSM(Isotripair)to sim-cbl3-3-lap-out by ME. 2018062 Page39 Reserve PCIe circuit 2018062 Page39 Add R1814 for PU DEVSLP. 2018062 Change connector Isotripair by ME. 2018062 Page 29 Change connector P11 Isotripair by ME, add PLURLP3 for EMI. 2018062 Page31 Del CN18 by ACER. 2018062 Page31 Add PR109-PR177 for power breakdown. 2018062 Page18 Del R106,R166,R204, R065 by ACER. 2018062 Page21 change K8-con CN13 to 24pin first by ACER. 2018062 Page27 Add Hole and SWH for BATT_FEM. 2018062 Page21 Add P113 by ACER. 2018062 Page26 Add R1815. 2018062 Page21 change K8-con CN13 to 24pin first by ACER. 2018062 Page311 Add IPJ12. 20180621 Page34 change PCAPC72 from 7343 to 3528. 20180621 Page21: Reserve D18 for SMT_DET. 20180621 Page26: Change CN2 from 28 to 24 pins for LEDR. 20180621 Page22: Del R6R7LED1, move to LEDR. 20180621 Page1:3: Reserve NXP resistor R1016-R1019. 20180624 Page21 Add R1828. 20180624 Page39 Add PR173. 20180624 Page21 swap CN13 pin define. 20180625 Page21 swap CN8 pin define by ME. 20180625 Page27 Add Hall IC by ME. 20180625 Page28 change CN2 from 24 to 20pin. 20180625 Page28 add diode D29 and R1824 for LID_OPEN_L for leakage issue 20180625 Page21-add R1821 by Asmt. 20180625 Page21 swap CN12 pin define by ME. 20180627 Page31 change V4 solution by ACER. 20180627 Page28 USB remove ,+mATA power connect to PP3300_DX. 20180627 Page21 U13 remove, power source pass through to output. 20180627 Page21 Add PR174, reserve PR175,PR176 to input port of P14 by ACER. 20180627 Page28 set Bat_LED+-(spin mode)1,U16 PWRLED+-!N11, Battery LED0--R2, PWRLED0--R1 20180627 Page21 U13 pin 1--+BWDT2, pin 6--+COL3(113 key) 20180627 Page21 swap sst RLZ2-suff file & R241. 20180628 Page21 Add R1825 20180628 Page28 Remove +-V_RTC interconnect 20180628 Page41 Remove/reserve -SMDOR_VREF_DQ0 interheat 20180628 Page31 Remove/reserve -SMDOR_VREF_DQ1 interheat 20180628 Page31 Remove -V2,V3,V4,V5,V6,V7,V8,V9,V10,V11,V12,V13,V14,V15,V16,V17,V18,V19,V20,V21,V22,V23,V24,V25,V26,V27,V28,V29,V30,V31,V32,V33,V34,V35,V36,V37,V38,V39,V40,V41,V42,V43,V44,V45,V46,V47,V48,V49,V50,V51,V52,V53,V54,V55,V56,V57,V58,V59,V60,V61,V62,V63,V64,V65,V66,V67,V68,V69,V70,V71,V72,V73,V74,V75,V76,V77,V78,V79,V80,V81,V82,V83,V84,V85,V86,V87,V88,V89,V90,V91,V92,V93,V94,V95,V96,V97,V98,V99,V100,V101,V102,V103,V104,V105,V106,V107,V108,V109,V110,V111,V112,V113,V114,V115,V116,V117,V118,V119,V120,V121,V122,V123,V124,V125,V126,V127,V128,V129,V130,V131,V132,V133,V134,V135,V136,V137,V138,V139,V140,V141,V142,V143,V144,V145,V146,V147,V148,V149,V150,V151,V152,V153,V154,V155,V156,V157,V158,V159,V160,V161,V162,V163,V164,V165,V166,V167,V168,V169,V170,V171,V172,V173,V174,V175,V176,V177,V178,V179,V180,V181,V182,V183,V184,V185,V186,V187,V188,V189,V190,V191,V192,V193,V194,V195,V196,V197,V198,V199,V200,V201,V202,V203,V204,V205,V206,V207,V208,V209,V210,V211,V212,V213,V214,V215,V216,V217,V218,V219,V220,V221,V222,V223,V224,V225,V226,V227,V228,V229,V230,V231,V232,V233,V234,V235,V236,V237,V238,V239,V240,V241,V242,V243,V244,V245,V246,V247,V248,V249,V250,V251,V252,V253,V254,V255,V256,V257,V258,V259,V260,V261,V262,V263,V264,V265,V266,V267,V268,V269,V270,V271,V272,V273,V274,V275,V276,V277,V278,V279,V280,V281,V282,V283,V284,V285,V286,V287,V288,V289,V290,V291,V292,V293,V294,V295,V296,V297,V298,V299,V300,V301,V302,V303,V304,V305,V306,V307,V308,V309,V310,V311,V312,V313,V314,V315,V316,V317,V318,V319,V320,V321,V322,V323,V324,V325,V326,V327,V328,V329,V330,V331,V332,V333,V334,V335,V336,V337,V338,V339,V340,V341,V342,V343,V344,V345,V346,V347,V348,V349,V350,V351,V352,V353,V354,V355,V356,V357,V358,V359,V360,V361,V362,V363,V364,V365,V366,V367,V368,V369,V370,V371,V372,V373,V374,V375,V376,V377,V378,V379,V380,V381,V382,V383,V384,V385,V386,V387,V388,V389,V390,V391,V392,V393,V394,V395,V396,V397,V398,V399,V400,V401,V402,V403,V404,V405,V406,V407,V408,V409,V410,V411,V412,V413,V414,V415,V416,V417,V418,V419,V420,V421,V422,V423,V424,V425,V426,V427,V428,V429,V430,V431,V432,V433,V434,V435,V436,V437,V438,V439,V440,V441,V442,V443,V444,V445,V446,V447,V448,V449,V450,V451,V452,V453,V454,V455,V456,V457,V458,V459,V460,V461,V462,V463,V464,V465,V466,V467,V468,V469,V470,V471,V472,V473,V474,V475,V476,V477,V478,V479,V480,V481,V482,V483,V484,V485,V486,V487,V488,V489,V490,V491,V492,V493,V494,V495,V496,V497,V498,V499,V500,V501,V502,V503,V504,V505,V506,V507,V508,V509,V510,V511,V512,V513,V514,V515,V516,V517,V518,V519,V520,V521,V522,V523,V524,V525,V526,V527,V528,V529,V530,V531,V532,V533,V534,V535,V536,V537,V538,V539,V540,V541,V542,V543,V544,V545,V546,V547,V548,V549,V550,V551,V552,V553,V554,V555,V556,V557,V558,V559,V560,V561,V562,V563,V564,V565,V566,V567,V568,V569,V570,V571,V572,V573,V574,V575,V576,V577,V578,V579,V580,V581,V582,V583,V584,V585,V586,V587,V588,V589,V590,V591,V592,V593,V594,V595,V596,V597,V598,V599,V600,V601,V602,V603,V604,V605,V606,V607,V608,V609,V610,V611,V612,V613,V614,V615,V616,V617,V618,V619,V620,V621,V622,V623,V624,V625,V626,V627,V628,V629,V630,V631,V632,V633,V634,V635,V636,V637,V638,V639,V640,V641,V642,V643,V644,V645,V646,V647,V648,V649,V650,V651,V652,V653,V654,V655,V656,V657,V658,V659,V660,V661,V662,V663,V664,V665,V666,V667,V668,V669,V670,V671,V672,V673,V674,V675,V676,V677,V678,V679,V680,V681,V682,V683,V684,V685,V686,V687,V688,V689,V690,V691,V692,V69